



Temperature-Dependent Carrier Transport in GaN Nanowire Wrap-Gate Transistor

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Abstract: For the creation of next-generation nanoscale devices, it is crucial to comprehend the carrier transport mechanisms in nanowires. Here, we examine how temperature affects the properties of GaN nanowire wrap-gate transistors (WGTs), which are made via a top-down technique. The predicted conductance in this transistor remains essentially unaltered up to a temperature of 240 K and then increases after that as the temperature rises. This is true for increasing temperature at gate voltages less than threshold voltage ($V_{gs} < V_{th}$). Sharp fluctuations happen when the temperature rises with a gate voltage of $V_{th} < V_{gs} < V_{FB}$. The conductance steadily decreases with increasing temperature after increasing the gate bias to $V_{gs} > V_{FB}$. These phenomena are possibly attributed to phonon and impurity scattering processes occurring on the surface or core of GaN nanowires.

Keywords: wrap-gate transistor; nanowire; GaN; surface/core; carrier scattering



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1. Introduction

Due to their potential usage in next-generation, high-performance electronic and optoelectronic devices, nanoscale circuit elements such as semiconductor-based nanowires have undergone significant development [1–12]. For example, nanowires can significantly shrink field-effect transistor (FET) geometries. As with FET, Fin-FET, tri-gate, omega gate, and gate-all-around (GAA) or wrap-gate (WG) devices, the scaling of various transistor types depends on geometries [13–21]. Due to their superior electrostatic controls, WG-based devices produce exceptionally impressive results when compared to alternative architectures. In comparison to the conventional technique (i.e., bottom-up), top-down device production of nanowire-based WG transistors (WGTs) has many advantages, including reduced device size, an orderly alignment of nanowires in a parallel pattern, and a high yield is attainable at a large scale. Device performance in high-speed, high-power, high-frequency, and high-temperature applications is superior for GaN-based nanowire devices. With a high I_{on}/I_{off} ratio, a tiny gate leakage, and a high conductance, a GaN nanowire-based device can regulate its normally-off state. This work involved the top-down fabrication of a device and an investigation of the carrier transport mechanism in a GaN nanowire WGT on a GaN-on-insulator (GaNOI) substrate.

The operation of nanowire devices at cryogenic temperatures is particularly interesting since, at ambient temperatures, nanowire devices do not provide comprehensive information about their electronic transport. It is possible to identify distinct conduction

pathways thanks to the temperature dependence of the current-voltage (I - V) properties of nanowires. The idea of impurity or Coulomb scattering and electron-phonon scattering on the surface/core of nanowires was developed after a thorough understanding of the role of carrier scattering in semiconductor nanowires.

In earlier studies, we exclusively studied the static (dc) performance of a GaN nanowire WGT at room temperature, as well as the effects of surface/core traps, architecture, and other factors [22–24]. Here, we have explored the effect of temperature on the gate bias-dependent carrier transport mechanism in the GaN nanowire WGT to determine how the GaN nanowire's conductance varies. When the gate voltage was low (below the threshold voltage), the conductance decreased and subsequently increased with temperature, but when the gate voltage was high, the conductance decreased monotonically as the temperature increased. Carrier scattering mechanisms, such as electron-phonon and impurity scattering, can be used to explain these discrepancies.

2. Materials and Methods

We employed a GaNOI substrate from SOITEC Corporate that was manufactured using the Smart Cut™ process and double-wafer transfer technology for the GaN nanowire WGT architecture. A GaN layer (150 nm thick) and buried oxide (SiO₂, 800 nm thick) are both present on a sapphire (0.65 mm thick) substrate to form a 4-inch diameter GaNOI substrate. To begin, the crystal orientation $\langle 11\text{-}20 \rangle$ was etched on the GaNOI substrate using an advanced electron beam (e-beam) lithography tool and PMMA resist. The GaN film was selectively etched using an inductively coupled plasma dry etching technique, and then the device-patterned wafer was etched with a TMAH solution for 10 min at 90 °C. Instead of the vertical c -plane (0001) crystal direction, this etchant solution only etches in the lateral crystal direction. This etchant decreased the GaN film width in the crystal direction $\langle 11\text{-}00 \rangle$, resulting in 83 nm heights with corresponding triangular sidewall orientations $\langle 11\text{-}01 \rangle$. To remove the buried oxide beneath the GaN nanowires effectively, the substrate was rinsed in a buffer-oxide etchant (BOE) solution.

Additionally, on the GaN pattern, selectively develop undoped GaN (50 nm thick) and AlGaIn (20 nm thick) films using the metal-organic chemical vapor deposition (MOCVD) technique. Here, the patterned GaN film served as the r -plane for a self-limiting re-grow process in the $\langle 11\text{-}01 \rangle$ orientation. It is quite impressive that the surface of the r -plane contains nitrogen (N) atoms that were simply interacting with hydrogen (H) atoms in the MOCVD chamber and generating N-H bonds, which enhanced stability and limited growth in the plane direction [22]. AlGaIn/GaN films could so readily be formed again, though only on the source and drain regions and not on the GaN nanowire. This procedure prevented the GaN nanowire's area from changing. Re-grown AlGaIn/GaN films are crucial in this situation because they reduce series resistance by utilizing the two-dimensional electron gas (2DEG) region at the interface to the source/drain sections.

With the help of the plasma-enhanced atomic layer deposition (PE-ALD) technique, gate metal (TiN, 10 nm thick) and high- k gate oxide (Al₂O₃, 20 nm thick) were gradually coated for the construction of WGT devices. As a result, a four-layer metallization scheme (Ti/Al/Ni/Au) was deposited as source/drain regions using the e-beam approach, followed by rapid thermal annealing in a N₂ environment at 850 °C for 30 s. Finally, a gate metal layer made of Ni/Au was coated to serve as an external contact for electrical properties. Using a Hall-effect measurement device (HL5500PC, Nanometrics), the concentration and mobility of the regrown AlGaIn film, $9.75 \times 10^{12} \text{ cm}^{-2}$ and $1630 \text{ cm}^2/\text{V}\cdot\text{s}$, were assessed. A field-emission tunneling electron microscope (FE-TEM, JEM-2100F) analysis of the device architecture was performed. A Keithley source (4200-SCS) linked to an MST-6VC vacuum chamber with a low-temperature control system was used to measure the device's temperature-dependent I - V properties. The temperature control system has a sensitivity of $\pm 1 \text{ K}$.

3. Results

The investigated GaN nanowire WGT device's schematic architecture is shown in Figure 1a (on the left). It has a gate length of $2\ \mu\text{m}$ and 64 triangular-shaped one-dimensional nanowires with identical $\langle 1-101 \rangle$ crystal facets on each of its two faces. The right side of Figure 1a displays a crystal-clear FE-TEM image of a triangular-shaped GaN nanowire core surrounded by gate oxide and gate metal. Figure 1b displays the drain current (I_{ds}) vs. gate voltage (V_{gs}) curves of the AlGaIn/GaN-based GaN nanowire WGT as a function of temperature, with increments of 30 K between 130 and 310 K for the drain voltage (V_{ds}) of 0.1 V. As can be seen, the drain leakage current demonstrates a distinct temperature dependence, rising from 1.12×10^{-13} A at 130 K to 2.15×10^{-12} A at 310 K. The increase in drain leakage current might be driven by surface-related traps and tunneling mechanisms that are facilitated by temperature [25,26].

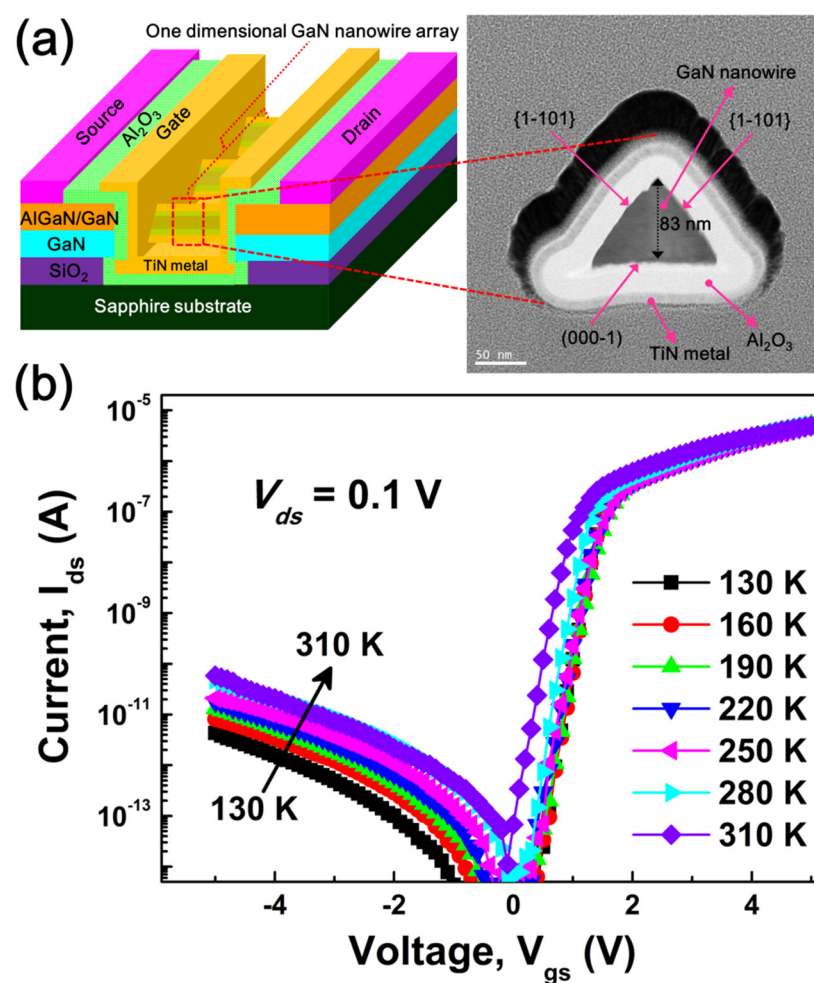


Figure 1. (a) Schematic device architecture of the fabricated GaN nanowire WGT with a high-resolution FE-TEM cross-section image of a triangular-shaped GaN nanowire. (b) Logarithmic plots of drain current (I_{ds}) versus gate voltage (V_{gs}) at $V_{ds} = 0.1$ V as a function of temperature.

The linear properties of I_{ds} versus V_{gs} of GaN nanowire WGT as a function of temperature are depicted in Figure 2a. GaN WGT operates typically with a positive threshold voltage (V_{th}) and a maximum drain current ($I_{d,max}$) of $6\ \mu\text{A}$ at all temperatures. The inset of Figure 2a depicts how V_{th} changes as a function of temperature. The V_{th} reduces with temperature in general, but a small variation reveals that the V_{th} declines up to the critical temperature (i.e., 160 K), reaches its maximum value at 190 K, and then rapidly decreases with temperature. Further research in the carrier transport of GaN nanowires is required

because the existence of the critical temperature is not currently well known. It is observed that when the temperature rises, the total V_{th} gradually decreases. This may be because the doping concentration in the nanowire channel decreases due to incomplete dopant ionization at low temperatures, where it exponentially decays and becomes smaller than the electron concentration [27].

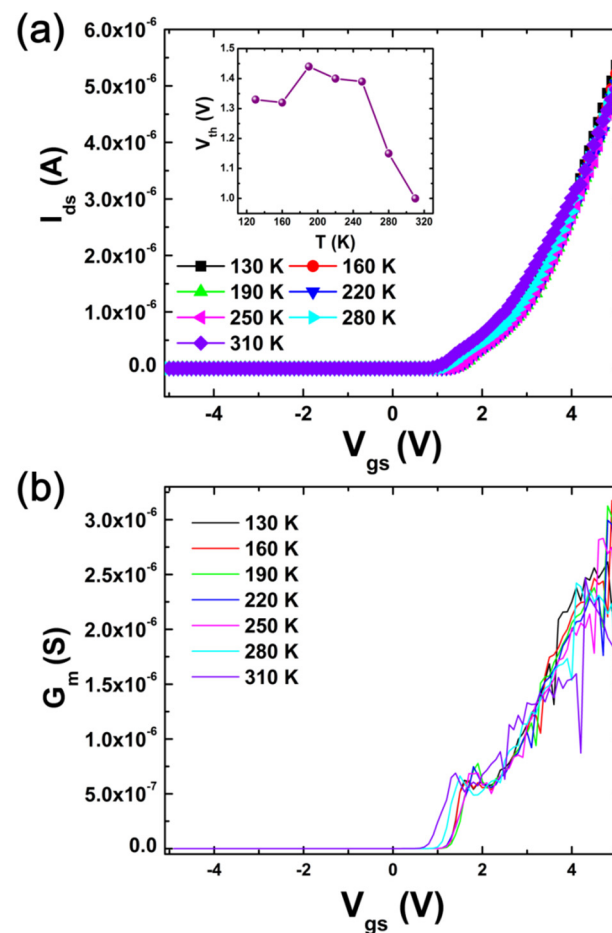


Figure 2. (a) Linear I_{ds} versus V_{gs} as a function of temperature and inset shows temperature dependence of threshold voltage; (b) G_m versus V_{gs} as function of temperature of the GaN nanowire WGT.

The device's G_m – V_{gs} properties are depicted in Figure 2b as a function of temperature. For all temperatures, the G_m increases with rising gate voltages, but there is a little variance at low gate voltages (1.4–1.9 V). This is due to the fact that surface channels open at specific gate voltages, such as 2 to 5 V, and that core channels open at low gate voltages (i.e., 1.4–1.9 V) [23]. Finally, surface channels become dominant at high gate voltages [23].

Using the conductance data on various gate biases could more precisely analyze the carrier transport process across the GaN nanowires. Notably, the G_m is falling while the V_{gs} is falling in Figure 3. This is brought on by the nanowire channel's carrier depletion at lower V_{gs} . At gate bias of $V_{gs} < V_{th} = 1.44$ V (Figure 3a), the G_m decreases and then increases with increasing temperature; at $V_{th} > V_{gs} = V_{FB}$ (i.e., $V_{FB} = 3.7$ V was evaluated from the capacitance-voltage characteristics of GaN nanowire WGT not shown here); and finally, at gate bias of $V_{gs} > V_{FB}$ (Figure 3c), the G_m abruptly decreases with increasing temperature.

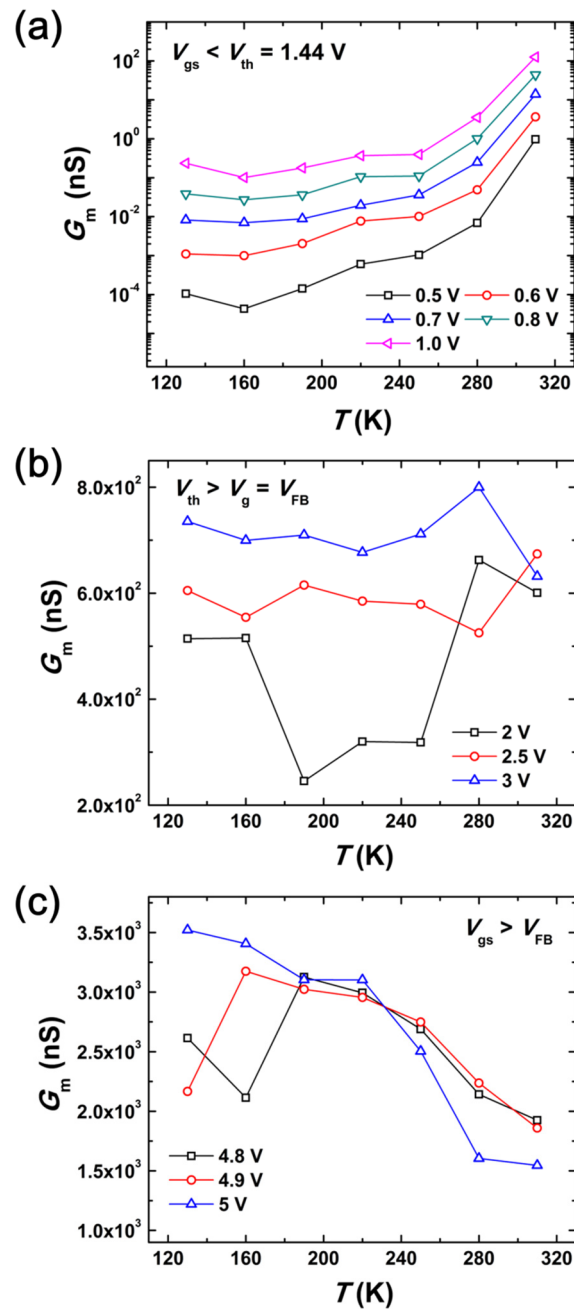


Figure 3. Gate voltage-dependent G_m versus T characteristics of the GaN nanowire WGT: (a) below threshold voltage; (b) between threshold voltage and flat band voltage; (c) above flat band voltage.

The carrier scattering mechanisms on the surface/core of the GaN nanowires can explain these characteristics. The values of G_m are high at 130 K and reach their lowest point at the critical temperature (160 K) for gate voltages of $V_{gs} < V_{th} = 1.44$ V. Thereafter, they grow quickly with rising temperatures. For the temperature-dependent conductance experiments, InAs nanowires showed a similar critical temperature (140 K) [19]. The typical response of the donor activation process to temperature is an increase in G_m with rising temperature. As the temperature drops, the donors become frozen, reflecting a fall in G_m . $G_m(T) = \sigma_C(T)(A/L_g)$, where $\sigma_C(T)$ is the temperature-dependent carrier conductivity, L_g is the gate length, and A is the nanowire cross section that can be used to indicate the temperature dependence of nanowire conductance. The temperature dependency of conductivity is represented as $\sigma_C(T) = [q^2 n(T) \tau(T) / m^*]$, where q is the charge, $n(T)$ is the temperature-dependent carrier density of GaN nanowire channels, m^* is effective mass, and

$\tau(T)$ is the relaxation time as a function of temperature. Here, the main kind of scattering mechanism is determined by the temperature-dependent relaxation time. In actuality, electron-phonon scattering is less likely when the phonons are frozen at low temperatures.

On the other hand, the data in Figure 3a demonstrates that conductance rises with applied V_{gs} (carrier density). The rise in conductance is normal behavior for a charged impurity scattering dominant situation. At this point, as conductivity rises, free carrier screening is intensified due to Coulombic (scattering) perturbation, which causes scattering time (also known as relaxation time, $\tau(T)$) to rise with carrier density. Defects, charge dislocations, and background contaminants all contribute to the potential for Coulombic scattering. Another factor could be the dual-wafer transfer method utilized to create the epitaxial GaNOI structure, which has the potential to reduce the crystal quality of the GaN layer [22].

The conductance fluctuates after the threshold voltage and up the flat band voltage (Figure 3b, $V_{th} > V_{gs} = V_{FB}$). This is a result of the complex temperature dependence of the product $n(T)\tau(T)$ caused by the interaction of charged impurities and phonon scattering, which causes a complex signature to occur in the conductivity. This suggests that surface donors in the GaN nanowire channel compensate for the core donors. Carriers remain fluctuating (i.e., $V_{gs} = 4.8$ and 4.9 V) at low temperatures, but rapidly drop with increasing temperature as $V_{gs} > V_{FB}$ (Figure 3c). It is important to note that at $V_{gs} = 5$ V, conductance rapidly declines without any issues.

Here, we need to think about two things: (i) low conductivity is shown in the relaxation time's sharp reduction with rising V_{gs} [23] and (ii) mobility reduces with rising temperature (i.e., inversely with resistance) [19]. These may be typical behaviors of the electron-phonon scattering contribution. Ultimately, we have come to the conclusion that optical electron-phonon scattering is possible at the nanowires' surfaces and that impurity scattering is possible in the core of GaN nanowires.

4. Conclusions

In summary, applied gate potentials were used to investigate the electrical characteristics and carrier transport mechanism in the surface/core of GaN nanowire WGTs. When determining the carrier scattering mechanisms on the surface/core of a GaN nanowire, fundamental properties such as G_m are crucial. The G_m increase with temperature at $V_{gs} < V_{th} = 1.44$ V was caused by impurity scattering that possibly occurred inside the GaN nanowire's core. At a gate bias of $V_{th} > V_{gs} = V_{FB}$, the values of G_m fluctuate because the core and surface currents in GaN nanowires balance one another. Then, G_m drops with temperature, possibly because of phonon scattering, which is important at the gate bias of $V_{gs} > V_{FB}$.

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Data Availability Statement: The data is available on reasonable request from the corresponding author.

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