IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 25 February 2026, accepted 18 March 2026, date of publication 20 March 2026, date of current version 25 March 2026.

Digital Object Identifier 10.1109/ACCESS.2026.3676370

RESEARCH ARTICLE

Enhanced DC Series Arc-Fault Detection in LVDC Systems With Capacitor-Assisted Impedance Shaping

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This work was supported by Korea Institute of Energy Technology Evaluation and Planning (KETEP) and the Ministry of Climate, Energy and Environment (MCEE) of the Republic of Korea under Grant RS-2024-00509127.

ABSTRACT A DC grid can achieve high power conversion efficiency by reducing conversion stages between DC energy resources and loads. However, as system complexity increases, DC distribution systems face series arc faults due to damaged power cables and loose connectors, which can induce a fire hazard. Unlike AC grids, DC grids lack natural current and voltage zero crossings, which complicates arc-fault detection. This paper investigates series arc fault detection in LVDC systems with auxiliary DC-link/feeder capacitance for impedance shaping. The proposed capacitor-assisted impedance shaping increases the magnitude of arc-induced current variation and strengthens the frequency-spectrum change of the line current used by the FFT-based detector, thereby improving DC series arc-fault detectability. The operational principle is analyzed to derive capacitance-based impedance-shaping design guidelines for such LVDC systems. Also, a hybrid detector combines time-domain and frequency-domain analyses to detect DC series arc faults, which utilizes the arc characteristics of DC and AC components. Experimental validation of the proposed structure and detection algorithm is performed on a 30-kW laboratory LVDC testbed.

INDEX TERMS Low voltage DC grid, DC grid, arc fault, fault diagnosis, impedance shaping, time-domain analysis, frequency-domain analysis.

I. INTRODUCTION

A DC-grid systems are gradually expanding, because it has high efficiency, low noise, and good connectivity with renewable energies and energy storage systems (ESS) [1], [2], [3]. With increasing of DC-grid systems, several standards have been developed in response to the growing interest in their safety and reliability in electrical problems [4], [5], [6]. DC series arc faults are a major fault type that occur because of damaged and aged power cables, loose connectors, and cracked solder joints. The National Electrical Code requires the installation of a series arc fault detection devices (AFDDs) of over 80 V [7]. In the application of photovoltaic (PV) systems, Underwriters Laboratories (UL) invented UL 1699 B standards to guarantee the AFDDs performance, which is only designed for PV systems [8]. The International Electrotechnical Commission (IEC) developed IEC 62606 for performance verification of AFDDs. Therefore, the DC series arc fault detection can improve the reliability and safety of DC-grid systems.

Various DC series arc fault detection algorithms have been introduced for DC systems. DC arc faults can occur in both series and parallel fault conditions. A parallel arc fault is the same as a short circuit condition, and can be easily detected

The associate editor coordinating the review of this manuscript and approving it for publication was Chuan Li.

by a large change in the current [9], [10]. However, a series arc fault has only a small current variation, because it operates as injection of series resistance in power line and connector. Therefore, a series arc fault is more challenging than parallel arc fault. DC series arc fault detection devices require high precision and fast detection speeds, because the energy losses in the arc fault are converted into heat energy. A DC series arc fault detection based on a time domain analysis was evaluated using voltage and current information [11], [12], [13]. These methods have a simple implementation with the characteristics of arc fault resistance. However, it is difficult to distinguish the arc fault condition and normal operation with small current variation. In addition, several sensors are required to improve fault detection precision compared to normal conditions [12]. In [14], [15], [16], [17], and [18], frequency domain analyses were performed using the current to determine the arc fault characteristics. In [15] and [16], the fast Fourier and wavelet transforms were used to extract the arc fault characteristics. In [17], the high-gain bandpass filter was introduced to amplify the fault signal. It considers the chaotic variation in the arc impedance, which can distinguish normal and fault conditions. However, the AC magnitude variation depends on the impedance design of the converter and inverter, which determines the precision of arc fault detection. In [18], a resonant filter was designed to modify the system impedance and achieve a high fault magnitude. However, auxiliary hardware increases the system cost and power losses. In [19], [20], and [21], hybrid arc fault detection methods employing time and frequency domain analyses were introduced to improve the detection precision. This increases the number of available parameters when using multi-domain analyses. In [19] and [20], statistical analyses in the time and frequency domains were performed to distinguish between normal and arc fault. However, it passively measures the AC current from the designed power systems, which makes it difficult to achieve a consistent fault detection performance. In [21], the energy variation in the time and frequency domain analysis was used to distinguish between normal and arc fault conditions. However, it required current and voltage sensors, which increases the cost of the AFDDs. In [22], [23], [24], [25], [26], and [27], arc fault detection methods using artificial intelligence were developed using both normal and fault data. Those methods use several time and frequency domain characteristics, such as the average, root-mean square, min-max values, entropy, energy level variation, fast Fourier transform (FFT), and wavelet transformer. In [22], [23], and [24], machine learning methods, such as support vector machine and random forests, were employed to detect arc faults from the accumulated datasets. Deep learning methods were used in [25], [26], [27], [28], and [29] to detect arc faults with various techniques. Preprocessing and proper feature extraction can improve the fault detection precision. Signal processing methods, such as time domain analysis, frequency domain analysis, and artificial intelligence, passively measure fault signals using a current transformer and Rogowski coil, which are decoupled from the power conversion. However, the signal processing methods require the chaotic AC current variation to detect the fault condition. However, the magnitude of the arc fault signal differs depending on the impedance of DC systems, such as power converter, and the line impedance. In addition, the conventional methods were focused on the arc fault detection between power sources and power conversion systems for the PV applications, which does not consider the complex interconnection of grid systems.

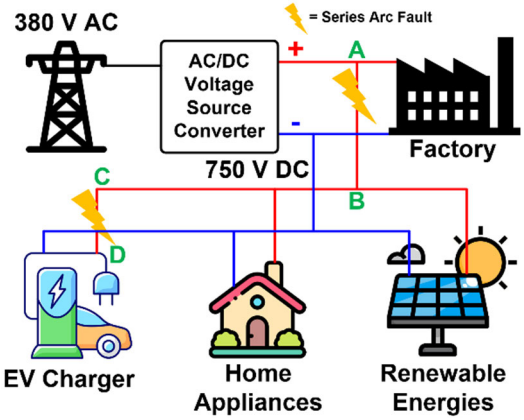

FIGURE 1. Example structure of LVDC systems.

The low voltage DC (LVDC) systems have complex inter-connection with renewable energy resources and electric loads [30], [31], [32]. Fig. 1 shows the distributed LVDC power systems, which includes the PV systems, ESSs, and loads. The arc faults can be occurred at the power line and connectors. The conventional AFDDs use the magnitude variation of frequency spectrum using AC components of current, because the AC components of arc resistance have chaotic variation. However, the precision of fault detection is different according to the impedance of grid systems. When the DC-Link voltage and current are unipolar 750 V and 40 A, Fig. 2 (a)-(c) shows the measured current at the normal and arc faults with inductive, capacitive, and resistive load impedances. The arc voltage and DC current have different time and frequency domain characteristics according to the load impedance, which determines the difficulty of fault detection. This verifies that strategic load impedance design can significantly enhance the detectability of series arc faults. This paper investigates the arc fault characteristics according to the grid impedance. The load impedance design makes it easy to classify the normal and arc faults. The coordinated time and frequency domain analysis uses the arc fault characteristics of DC and AC components. The experimental results show the performance of series arc fault detection with designed grid impedance and arc fault detection algorithm through 30-kW lab scale test-bed.

II. LVDC SYSTEMS FOR DC SERIES ARC FAULT DETECTION

A. CHARACTERISTICS OF ARC RESISTANCE

The series arc fault condition can be described with several arc resistance models, such as Stokes-Oppenlander

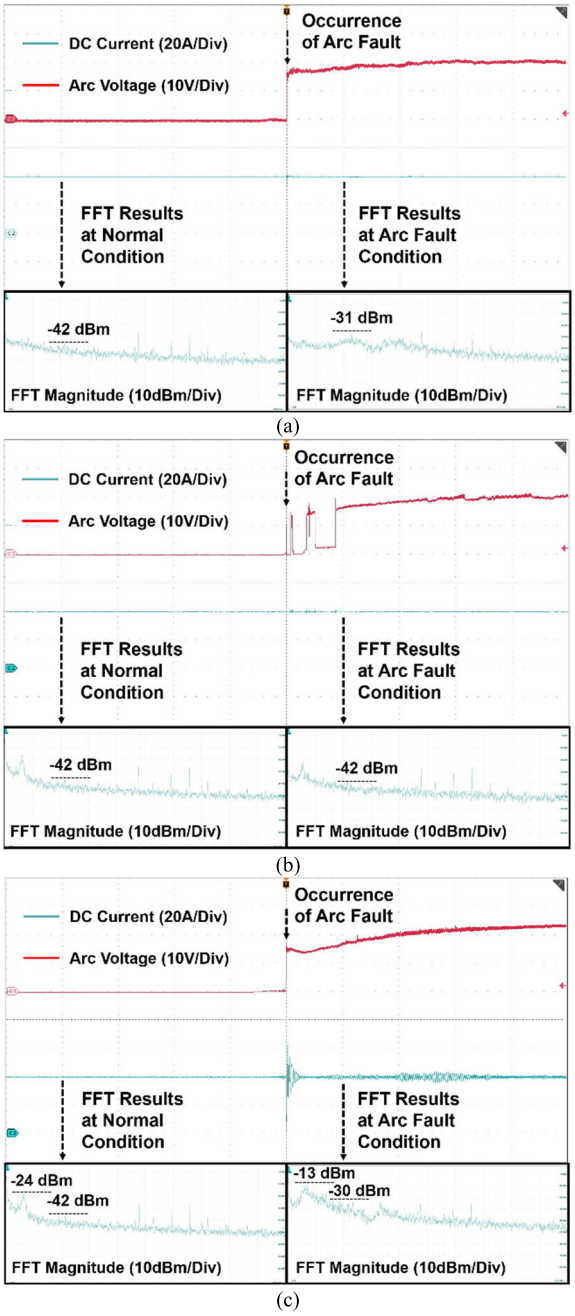

FIGURE 2. Experimental results of DC series arc fault conditions: (a) resistive load impedance (18 Ω), (b) inductive line impedance (1.65 mH), (c) capacitive load impedance (2.15 mF).

incident energy, Mayr-Cassie, and Nottingham [33], [34]. For example, Stokes/Oppenlander incident energy model can be derived as follows:

$$R_{arc} = \left(20 + 0.534 \cdot Z_g\right) / I_{dc}^{0.88} \tag{1}$$

where Z_g is the gap length of electrode, I_{dc} is the DC current. Differentiating (1) with respect to I_{dc} can obtain the negative resistance characteristics, as follows:

$$\frac{dR_{arc}}{dI_{dc}} = -0.88 \frac{20 + 0.534 Z_g}{I_{dc}^{1.88}} < 0 \tag{2}$$

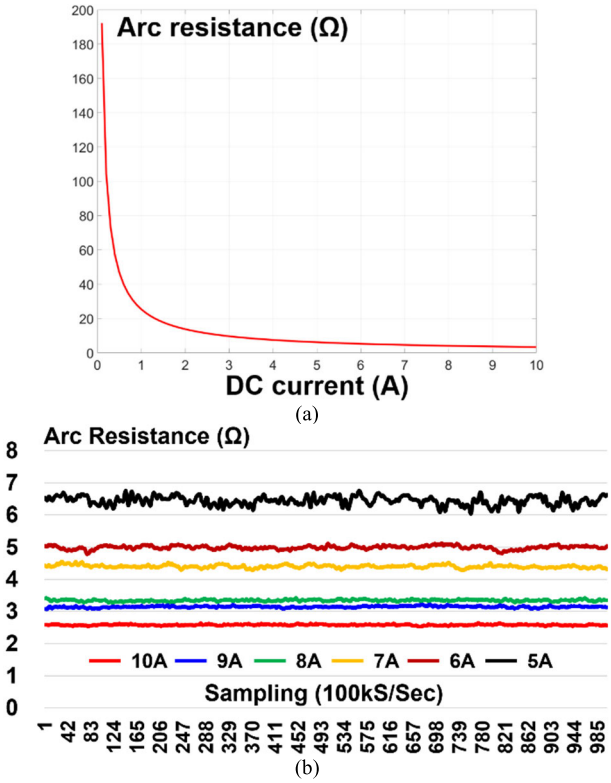

FIGURE 3. Arc resistance according to DC current: (a) theoretical model, (b)experimental results.

It increases the arc resistance with reduction of DC current, vice versa. Fig. 3 (a) shows the theoretical resistance of arc fault condition, which is verified through the experimental results of Fig. 3 (b). The small DC current increases the arc resistance. Therefore, the series arc fault condition reduces the load side DC-link voltage compared with normal condition at the same DC current level, which can be derived as follows:

$$V_{Link} = V_{Link,P} - R_{line} I_{dc} \tag{3}$$

$$V_{Link} = V_{Link,P} - \left(R_{line} + R_{arc}\right) I_{dc} \tag{4}$$

where V_{Link} is the measured voltage, $V_{Link,p}$ is the voltage of previous DC-link capacitor, R_{line} and R_{arc} are the line and arc resistances, respectively. When the arc fault occurs, Fig. 2 shows the reduction of V_{Link} at the same DC current.

In terms of AC components, the arc fault has chaotic arc impedance variation, which increases the high frequency AC current. The magnitude variation of frequency spectrum can detect the fault condition. When the DC current flows from DC link to feeder, the equivalent circuit can be described as Fig. 4. The arc-induced AC current component can be derived as follows:

$$i_{ac} = \frac{V_{Link,P} - V_{Link}}{r_{arc} + Z_{line} + Z_L} \tag{5}$$

where r_{arc} is the small-signal AC component of arc resistance, Z_{line} and Z_L are line and load impedances, respectively. From (5), the grid impedance is affected to the magnitude of

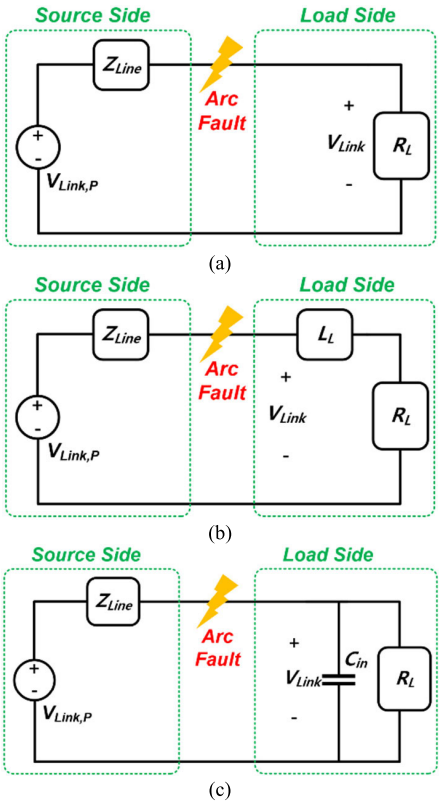

FIGURE 4. Equivalent circuit from DC link to feeder: (a) resistive load condition, (b) inductive line impedance, (c) capacitive load condition.

AC components. Fig. 4 (a) shows the resistive load impedance condition, which includes small line inductance and resistance (1.04 μH and 0.013 Ω). From Fig. 4 (a) structure, Fig. 2 (a) shows the experimental results in terms of time domain and frequency spectrum. From (5), the AC current with resistive impedance can be derived as follows:

$$i_{ac} = \frac{V_{Link,P} - V_{Link}}{r_{arc} + Z_{line} + R_L} \tag{6}$$

where R_L is the load resistance, respectively. When the Z_{line} is small to negligible, the magnitude of AC current is determined with arc and load resistances. In addition, the magnitude of AC current can be distinguished to classify the normal and arc faults with frequency domain analysis as shown in Fig. 2 (a). The series arc fault condition with inductive load impedance can be described with Fig. 4 (b). From (5), the AC current can be derived with large load inductance, as follows:

$$i_{ac} = \frac{V_{Link,P} - V_{Link}}{r_{arc} + Z_{line} + Z_L + R_L} \tag{7}$$

where Z_L is the impedance of load inductance. The Z_L has the large impedance as increase of frequencies, which reduces the magnitude of AC current. Fig. 2 (b) shows the experimental results of inductive load condition. It makes difficult to detect the arc fault condition with frequency domain analysis. The series arc fault condition with capacitive load impedance can be described in Fig. 4 (c).

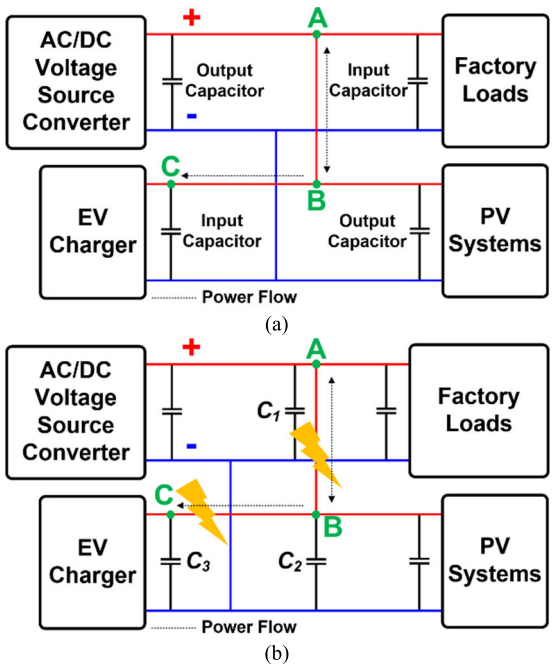

FIGURE 5. LVDC grid systems for arc fault detection: (a) conventional system structure, (b) proposed impedance based grid systems.

From (6), the AC current can be derived with large capacitive load as follows:

$$i_{ac} = \frac{V_{Link,P} - V_{Link}}{r_{arc} + Z_{line} + Z_C//R_L} \tag{8}$$

where Z_c is the impedance of load capacitance. The large Z_c reduces the impedance as increase of frequencies. It increases the magnitude of AC current at the arc fault as shown in Fig. 2 (c). Therefore, the capacitive DC-grid configuration is proper to detect the DC series arc fault condition through the signal processing method.

B. PROPOSED SYSTEM STRUCTURE FOR FAULT DETECTION

The capacitive load impedance is required to maximize the magnitude of AC current for using AC components of arc resistance. Fig. 5 shows the conventional and proposed LVDC grid structure. The conventional systems only consider the input and output capacitors of power conversion systems, as shown in Fig. 5 (a). However, the proposed structure includes the additional capacitors to detect the series arc fault condition though the signal processing method, as shown in Fig. 5 (b). When the arc fault occurs between point A and B, it should consider the bidirectional power flow with renewable energies and ESSs. When power flows from A to B, the C_1 regulates DC-link voltage. The C_2 operates as the load capacitor. When the power flows from B to A, the C_2 regulates the DC-link voltage. The C_1 operates as the load capacitor. Therefore, the feeder with bidirectional power flow should consider the input and output capacitances. In addition, the arc fault condition between point B and C is analyzed to achieve the fault detection capability. Where C is the DC

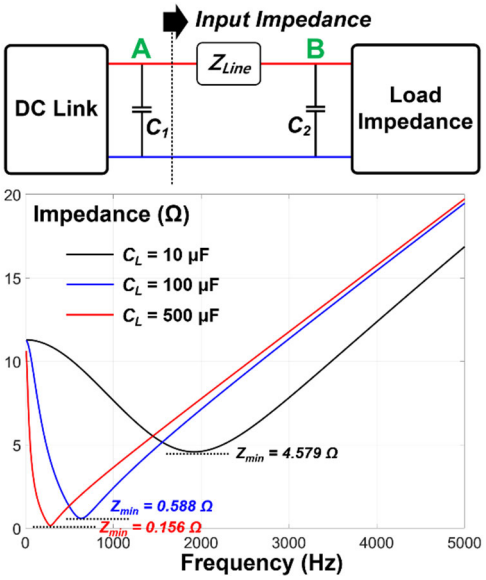

FIGURE 6. Input impedance variation according to load capacitor design.

loads, such as EV charger, home appliances, and factories. Since this condition is unidirectional power flow, the C_3 is effective to detect the arc fault between point B and C. The DC load requires the design of input capacitors for desired voltage regulation and hold-up times. The series arc fault detection capability can extend the considerations of input capacitance design. In addition, the location and values of auxiliary DC-link capacitors can be designed based on the line-impedance model.

The designed LVDC systems have 30-kW rated power. The cross-section area of power wire is 120 mm^2. The maximum line length between capacitors is designed as 300-meter. The parasitic components of power line are derived, as follows:

$$R_{line} = \rho L/A \tag{9}$$

$$L_{line} = \frac{\mu_o \mu_r L}{2\pi} \cdot \left\{ \ln\left(\frac{2L}{r}\right) - 1 \right\} \tag{10}$$

where ρ is resistivity of power line, L is the line length, A is the area of power line, μ_o is the permeability of free space, μ_r is the relative permeability of the wire material. From (9) and (10), the maximum R_{Line} and L_{Line} are 0.042 Ω and 630 μH with maximum line length, respectively. The AC current of capacitive systems can be derived with maximum R_{Line} and L_{Line}, as follows:

$$i_{ac} = \frac{V_{Link,P} - V_{Link}}{r_{arc} + R_{line} + j\omega L_{line} + \frac{R_L}{1+j\omega C_L R_L}} \tag{11}$$

Fig. 6 shows the input impedance between point B and C with 30-kW load condition according to selected capacitances. A sufficiently large load capacitance minimizes input impedance, enabling amplification of arc-related AC current components, which enhances detection sensitivity in signal processing. However, it requires a bulky capacitor bank, which reduces the power density and cost-effectiveness. From (11), the minimum capacitance can be designed with

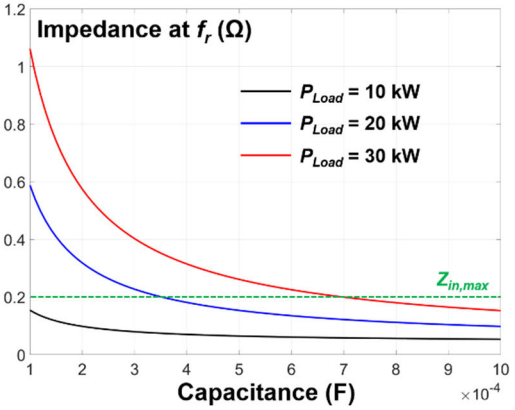

FIGURE 7. Input impedance according to load capacitance and power conditions.

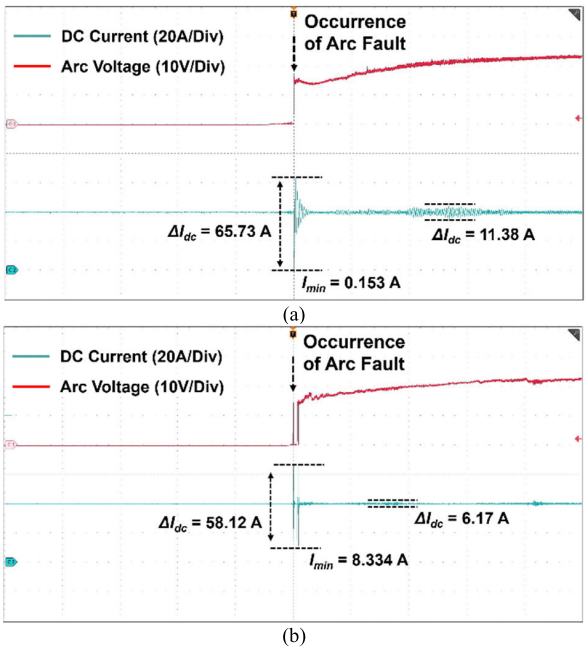

FIGURE 8. Experimental verification: (a) 1mF with 30 kW rated condition, (b)100 μF with 30 kW condition.

desired maximum load impedance at worst line impedance, as follows:

$$\frac{R_L}{1 + j\omega_{r,\min} C_L R_L} \le Z_{L,\max}\left(f_{r,\min}\right) \tag{12}$$

$$f_{r,\min} = \frac{1}{2\pi\sqrt{L_{line,\max} C_L}} \tag{13}$$

where $f_{r,min}$ is the minimum resonant frequency of L_{line} and C_L. From (12), the input impedance can be described as follows:

$$Z_{in} = R_{line} + j\omega_r L_{line} + Z_L\left(f_r\right) \le Z_{in,\max} \tag{14}$$

The required capacitance has variation according to the rated power condition, as shown in Fig. 7. It shows the desired C_L with worst power line condition. The increase of rated power condition requires the large capacitance to obtain the desired impedance, vice versa. Fig. 8 shows the experimental results

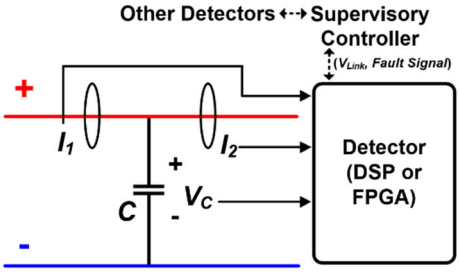

FIGURE 9. Sensing and processing structure for arc fault detection.

of magnitude variation of i_{ac} according to C_L values at the arc fault condition. It uses the 300-meter power line, DC power supply and electric load. Fig. 8 (a) shows the 1 mF case. In the arc fault transient, the variation and minimum value of current are 65.73 A and 0.153 A, respectively. The chaotic impedance variation of arc characteristics induces the fault current in stable arc conditions. In the stable arc, the current variation is 11.38 A. Fig. 8 (b) shows the 100 μF case. In the arc fault transient, the variation and minimum value of current are 58.12 A and 8.334 A, respectively. In the stable arc, the current variation is 6.17 A. From Fig. 8, the larger DC-link capacitor can achieve the smaller input impedance, which amplifies the arc fault characteristics. Thus, DC-link capacitors should be designed based on equations (12) and (13) to ensure a target input impedance that maximizes arc current variation for robust fault detection.

III. SERIES ARC FAULT DETECTION METHOD

The arc fault condition can be detected with the time and frequency domain analysis. Fig. 9 shows the designed DC-link capacitors with sensing structure for the arc fault detection. The digital signal processor (DSP) measures the DC-link voltage and DC current, which communicates with higher-level controller to share the DC-link voltage and fault signal. It is configured with a single DSP, single voltage and two current sensors. In terms of DC component of arc resistance, it reduces the DC-link voltage according to (1). The proposed fault detection uses the voltage variation of DC-link capacitor in time domain analysis. The DC-link voltage variation at the arc fault can be derived as follows:

$$\Delta V_{Link}\left(I_{dc}\right) = \left[V_{Link,P} - R_{line} I_{dc}\right] - \left[V_{Link,P} - \left(R_{line} + R_{arc}\right) I_{dc}\right] \quad (15)$$

From (15) and the arc-resistance model in (1), the DC-link voltage reduction due to a series arc fault can be approximated as $\Delta V_{Link} \approx I_{dc} R_{arc}$, which indicates that ΔV_{Link} increases with the DC current. The absolute voltage drop caused by the arc fault does not change drastically over the operating power range. However, as the load power increases, the natural ripple and noise components of the DC-link voltage also become larger because of converter dynamics and measurement noise. As a result, the effective detection margin tends to become smallest near the rated power. Therefore, the rated power condition is treated as the worst case when designing the

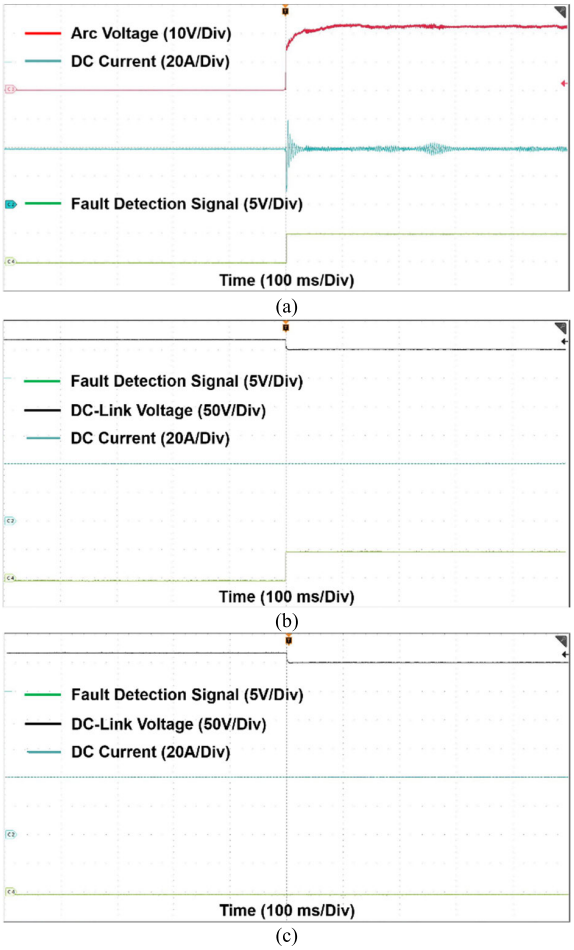

FIGURE 10. Arc fault detection using voltage analysis: (a) Arc fault condition using (16), (b) $V_{Link,P}$ variation using(16), (c) $V_{Link,P}$ variation using (17).

voltage-based threshold. From (15), the average of V_{link} can be calculated according to I_{dc}, as follows:

$$V_{Link,avg}\left(I_{dc}\right) = \frac{1}{K}\sum_{i=1}^{K} V_{Link}\left[I_{dc},\ i\right] \quad (16)$$

where K is the sampling number for averaging. From (16) and measured V_{Link}, the arc fault can be detected in time domain, as follows:

$$V_{Link,avg}\left(I_{dc}\right) - V_{Link}\left(I_{dc}\right) > V_{th} \quad (17)$$

From (17), it has simple detection algorithm. However, the V_{Link} has variation according to I_{dc} and $V_{Link,P}$, which increases the misdetection at normal condition. The arc fault detection can be improved with the measured $V_{Link,P}$, which requires communication with higher-level controller, as follows:

$$V_{Link,avg}\left(V_{Link,P},\ I_{dc}\right) - V_{Link}\left(V_{Link,P},\ I_{dc}\right) > V_{th} \quad (18)$$

However, it increases the complexity of arc fault detection, which has the trade-off relationship between the arc detection accuracy and system complexity. Fig. 10 is the experimental results with voltage variation in time domain analysis.

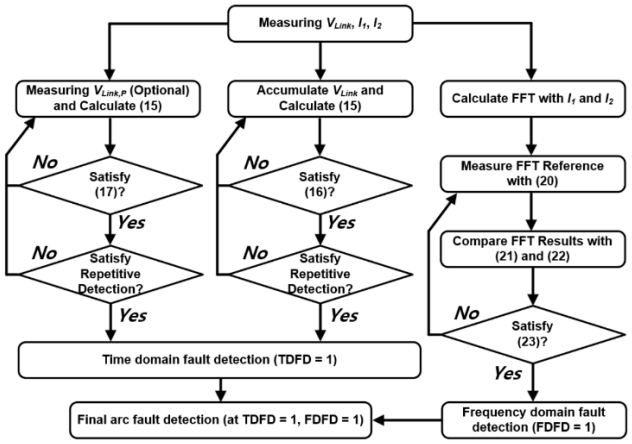

FIGURE 11. Flow chart for series arc fault detection.

Fig. 10 (a) shows the arc fault detection using (17). The DSP operates at a sampling frequency of 20 kHz. Accordingly, the voltage-based arc fault detection algorithm in (17) is executed every sampling period, enabling more than 20 detections within 1 ms. Fig. 10 (b) shows the $V_{Link,P}$ variation. It can not classify the arc fault and drastic $V_{Link,p}$ drop. Fig. 10 (c) shows the classification of $V_{Link,P}$ drop using (18). It verifies the trade-off relationship between the detection accuracy and detection complexity.

In terms of AC components, the arc resistance has chaotic variation, which increases the wide frequency spectrum of AC current. The impedance shaped grid reduces the load impedance at the designed frequency range. The proposed hybrid detection method utilizes FFT analysis of AC current components to distinguish normal and arc faults, complementing time-domain voltage analysis. The FFT results can be calculated with measured AC current, as follows:

$$I_{dc}[k,q] = \frac{1}{N}\left|\sum_{n=qN-N}^{qN-1} i_{dc}[n]\, e^{-2\pi kn/N}\right| \tag{19}$$

$$I_{dc}[k,j] = \frac{1}{N}\left|\sum_{n=jN-N}^{jN-1} i_{dc}[n]\, e^{-2\pi kn/N}\right| \tag{20}$$

where $I_{dc}[k]$ is the FFT results of DC current, q and j is the number of FFT results before and after the arc fault condition, N is the FFT size, n is the number of sampling point, which is from 0 to N. The FFT resolution is determined with the FFT size and sampling frequency. For example, when sampling frequency and FFT size are 20 kHz and 512, respectively, FFT resolution is 39 Hertz. When the number of FFT is 10, the calculation time for arc fault detection is over 256 ms. The maximum frequency of discrete Fourier transform is half of sampling frequency. The average of (19) can be calculated as a reference ($I_{dc,ref}$) for the normal operation, as follows:

$$I_{dc,ref}[k] = \frac{1}{P}\sum_{q=1-P}^{0} i_{dc}[k,q] \tag{21}$$

where P is the average number. The fault detector compares the FFT results of (20) with reference of (21), as follows:

$$I_{count}[k,j] = \begin{cases} 1, & at\ I_{dc}[k,j] > \alpha I_{dc,ref}[k] \\ 0, & at\ at\ I_{dc}[k,j] \le \alpha I_{dc,ref}[k] \end{cases} \tag{22}$$

where α is the threshold gain. The accumulated I_{count} can measure the magnitude difference of (19) and (20), as follows:

$$I_{comp}[j] = \sum_{k=k1}^{k2} I_{count}[k,j] \tag{23}$$

The comparison between (23) and threshold value (I_{th}) can detect the arc fault condition, as follows:

$$I_{comp}[j] > I_{th} \tag{24}$$

When (24) is satisfied, the arc fault is detected with FFT. To facilitate practical deployment, the impedance-shaping design in Section II-B can be directly mapped to detector configuration. Given the maximum feeder length L_{max} and cable information, the worst-case line parasitics $R_{Line,max}$ and $L_{Line,max}$ are obtained from (9)–(10), and the auxiliary DC-link/feeder capacitance C_L is then selected to satisfy the target input-impedance bound under the worst line condition using (12)–(14). The selected $\{L_{Line,max}, C_L\}$ further defines the minimum resonant frequency $f_{r,min}$ in (13), which indicates the frequency band where the capacitive grid most effectively reduces the input impedance and amplifies arc-induced AC current components.

Based on $f_{r,min}$, the DSP sampling frequency f_s and FFT size N are chosen to provide sufficient frequency resolution in the impedance-shaped band, and the detection latency is set by the FFT accumulation/averaging length P. Finally, the time-domain voltage threshold is calibrated at rated power as the worst case, while the FFT-domain thresholds (α, I_{th}) are set using the normal-operation reference $I_{dc,ref}$ defined in (21)–(24). Fig. 11 shows the flow chart of proposed arc fault detection through the capacitor voltage and current. The variation of DC-link voltage can detect the fault condition in terms of time domain analysis. The frequency spectrum change can detect the fault condition in terms of frequency domain analysis. When the fault is detected with both time and frequency domain analysis, the DSP transfers the arc fault detection flag to the higher-level controller. Two current sensors are placed at both sides of the DC-link capacitor as shown in Fig. 9. The downstream feeder current is used for (19)–(24), and the second sensor is used to validate abnormal current paths during disturbances.

The time-domain detector produces a fault indication when the averaged DC-link voltage criterion in (17) is satisfied under the repetitive-detection requirement in Fig. 11. The compensated criterion in (18) can be enabled when $V_{Link,P}$ is available. The frequency-domain detector produces a fault indication when the FFT-based condition in (24) is satisfied, based on the normal-operation reference $I_{dc,ref}$ in (21)–(22) and the comparison logic in (22)–(23). The arc-fault flag is

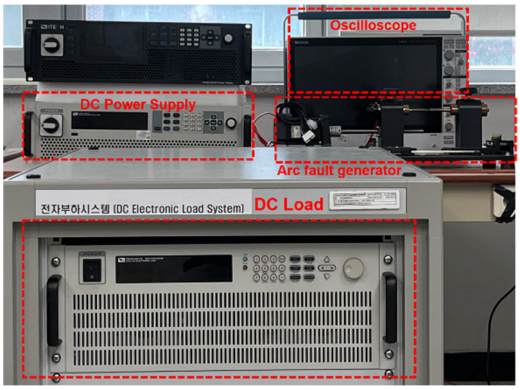

FIGURE 12. Experimental setups for arc fault detection.

TABLE 1. LVDC system and detector parameters.

parameters	values
P_{rated}	30 kW
V_{dc}, I_{dc}	750V, 40 A
$Cable/L_{max}$	120 mm^2, 300 m
$R_{line,max}$, $L_{line,max}$	0.042 Ω, 630 μH
C_L	700 uF
F_s	20 kHz
V_{th}	(17)-(18)
FFT Size, N	512
Frequency Resolution (Δf)	39 Hz
FFT decision gain (α)	(22)
FFT Threshold (I_{th})	(24)

transferred to the higher-level controller only when both the time-domain and frequency-domain indications are satisfied. If only the time-domain criterion is satisfied, the event is treated as a voltage-only anomaly and no trip is issued, while the FFT-based metric continues monitoring for confirmation. If only the frequency-domain criterion is satisfied, the event is treated as a spectrum-only deviation and no trip is issued, while the voltage criterion continues monitoring for confirmation. In both cases, the one-sided indication is cleared automatically when its own condition is not satisfied at subsequent checks or FFT updates. This two-stage confirmation rule reduces nuisance trips during non-fault disturbances.

IV. EXPERIMENTAL RESULTS

Fig. 12 shows the experimental setups to verify the performance of proposed capacitive LVDC systems and fault detection algorithm, which used power supply and DC load. The arc fault generator is designed with two copper electrodes, which is designed with UL 1699B standards. Also, the motor separates electrodes with designed arc gap-length and moving speed. The power line between the power source and load is 300 meters. The DC-link capacitor is designed with 700 μF for fault detection. Table 1 shows the key LVDC system parameters and the detector configuration, including capacitance values, worst-case line

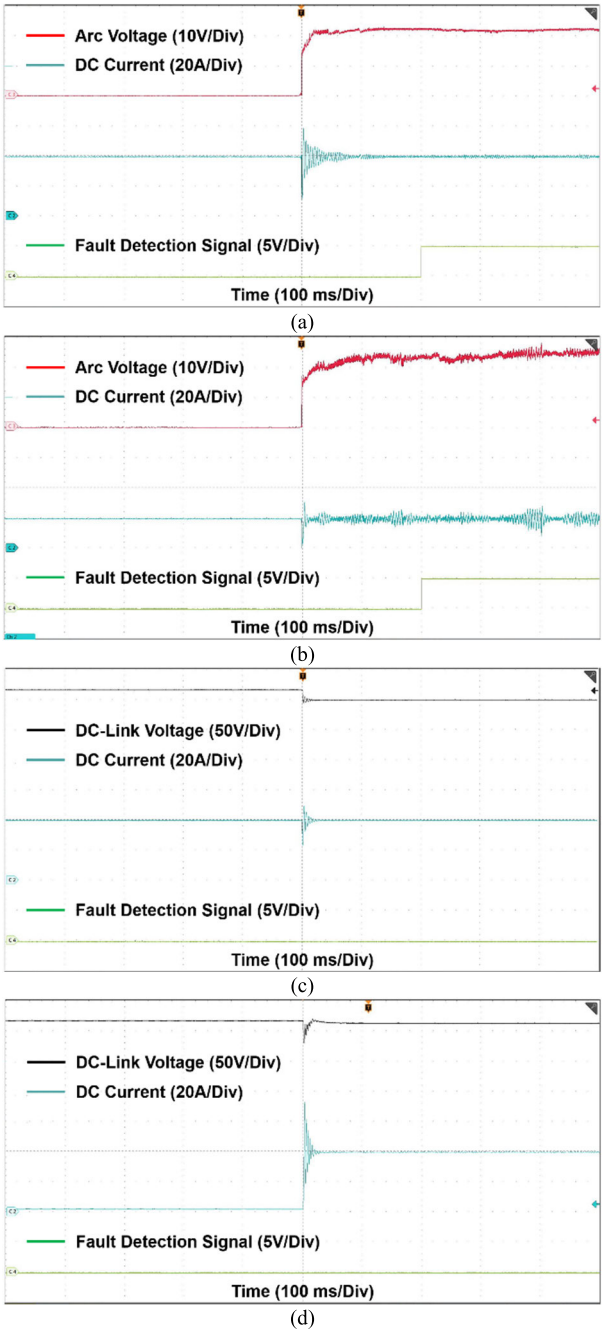

FIGURE 13. Arc fault detection using voltage analysis: (a) Arc fault condition with rated load, (b) Arc fault condition with mid load, (c)$V_{Link,P}$ variation, (d) Load current variation.

parameters, sampling/FFT settings, and decision thresholds for the time-domain and frequency-domain detectors.

Fig. 13 shows the experimental verification of series arc fault detection capability using proposed grid structure and algorithm. Fig. 13 (a) shows the series arc fault between DC-link voltage and load. The designed sampling speed is 20 kHz, which requires 25.6 ms for single FFT calculation. When the P is designed as 10, the calculation time of FFT is 256 ms to detect the fault condition. In addition, voltage-based fault detection requires only 1 ms. Therefore, the arc

fault detection speed is determined with frequency domain analysis. In the experimental results, designed method detects the arc fault condition within 270 ms. Fig. 13 (b) shows the series arc fault condition at the middle load. It also detected within 270 ms. Fig. 13 (c) shows the variation in DC link voltage. It can be classified as normal condition using the frequency domain analysis. Fig. 13 (d) shows the load current variation. It can be classified as normal condition using the time and frequency domain analysis. Therefore, the proposed capacitive DC grid is proper to detect the series arc fault condition using the designed fault detection algorithm. Fig. 8 shows the effect of capacitance variation, which uses 1 mF and 100 μF at 300-meter feeder line. The larger C_L reduces the input impedance, which increases the magnitude of arc current variation. Therefore, C_L can be selected with (12)-(13) to ensure sufficient margin under expected tolerances. The capacitor selection is based on the worst-case line parasitics at the maximum feeder length using (9)-(14). The immunity to common load transients using the experimental results is discussed in Fig. 10 and Fig. 13. Those cases show that typical DC-link voltage variation and load current variation are classified as normal.

A time-domain-only baseline declares a fault when the DC-link voltage condition in (17) is satisfied. This approach enables millisecond-level reaction because the computation is executed at every sampling instant. However, V_{Link} varies with operating conditions such as I_{dc} and $V_{Link,P}$, which can increase nuisance sensitivity under non-fault disturbances. This limitation is illustrated by the representative $V_{Link,P}$ variation case in Fig. 10 (b), where a voltage-only rule can be challenged without compensation. An FFT-only baseline declares a fault when the spectral criterion in (24) is satisfied. The decision latency is dominated by FFT windowing and accumulation. When f_s is 20 kHz and N is 512, one FFT window corresponds to 25.6 ms, and using ten consecutive FFT windows yields approximately 256 ms per decision update. The frequency-domain criterion is less affected by DC-link voltage disturbances in the representative case, as shown by the normal classification in Fig. 13(c). The coordinated detector asserts the trip flag only when both the voltage-based criterion and the FFT-based criterion indicate a fault as shown in Fig. 11. This two-evidence requirement rejects one-sided indications and explains why representative non-fault disturbances, including V_{Link} variation and load-current variation, are classified as normal in Fig. 13 (c)–(d), while arc faults are detected within 270 ms in the reported experiments.

V. CONCLUSION

The DC grid systems require high reliability and safety for stable operation. However, the DC series arc fault condition is difficult for detecting its failure, because it operates as the small arc resistance. In addition, the power line operates as a large inductance, which minimizes the fault characteristics. This paper proposes the capacitive DC grid to minimize the load impedance for arc fault detection. The proper capacitance selection and sensing structure are analyzed for classifying the normal and faults. In addition, the frequency and time domain analysis are coordinated with designed system structure. The experimental results can verify the performance of arc fault detection and classification of normal and arc faults.

REFERENCES

[1] T. Boonraksa, W. Pinthurat, P. Wongdet, P. Boonraksa, B. Marungsri, and B. Hredzak, "Optimal capacity and cost analysis of hybrid energy storage system in standalone DC microgrid," *IEEE Access*, vol. 11, pp. 65496–65506, 2023.

[2] R. Dey and S. Nath, "Cooperative active power management in multi-frequency microgrid with an energy storage system based on distance of source to load," *IEEE Access*, vol. 10, pp. 120398–120411, 2022.

[3] U. T. Salman, F. S. Al-Ismail, and M. Khalid, "Optimal sizing of battery energy storage for grid-connected and isolated wind-penetrated microgrid," *IEEE Access*, vol. 8, pp. 91129–91138, 2020.

[4] G. Li, J. Liang, T. Joseph, T. An, J. Lu, M. Szechtman, B. R. Andersen, and Q. Zhuang, "Feasibility and reliability analysis of LCC DC grids and LCC/VSC hybrid DC grids," *IEEE Access*, vol. 7, pp. 22445–22456, 2019.

[5] S. S. Khan and H. Wen, "A comprehensive review of fault diagnosis and tolerant control in DC–DC converters for DC microgrids," *IEEE Access*, vol. 9, pp. 80100–80127, 2021.

[6] B. R. Shrestha, U. Tamrakar, T. M. Hansen, B. P. Bhattarai, S. James, and R. Tonkoski, "Efficiency and reliability analyses of AC and 380 v DC distribution in data centers," *IEEE Access*, vol. 6, pp. 63305–63315, 2018.

[7] *NFPA70, National Fire Protection Association*, National Electrical Code (NEC), Quincy, MA, USA, 2011.

[8] *Outline of Investigation for Photovoltaic (PV) DC Arc-Fault Circuit Protection*, Underwriters Laboratories (UL) 1699B, Northbrook, IL, USA, Jan. 2013, no. 2.

[9] R. Fu and K. C. Montross, "A new method of coordinating ZCBs and fuses for a reliable short-circuit protection in DC power networks," *IEEE Access*, vol. 10, pp. 63270–63279, 2022.

[10] S. Teng, Z. Zhang, and L. Xiao, "Research on a novel DC circuit breaker based on artificial current zero-crossing," *IEEE Access*, vol. 8, pp. 36070–36079, 2020.

[11] H.-P. Park, M. Kim, J.-H. Jung, and S. Chae, "Series DC arc fault detection method for PV systems employing differential power processing structure," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 9787–9795, Sep. 2021.

[12] Q. Lu, Z. Ye, M. Su, Y. Li, Y. Sun, and H. Huang, "A DC series arc fault detection method using line current and supply voltage," *IEEE Access*, vol. 8, pp. 10134–10146, 2020.

[13] A. Shekhar, L. Ramírez-Elizondo, S. Bandyopadhyay, L. Mackay, and P. Bauera, "Detection of series arcs using load side voltage drop for protection of low voltage DC systems," *IEEE Trans. Smart Grid*, vol. 9, no. 6, pp. 6288–6297, Nov. 2018.

[14] W. Miao, Z. Wang, F. Wang, K. H. Lam, and P. W. T. Pong, "Multi-characteristics arc model and autocorrelation-algorithm based arc fault detector for DC microgrid," *IEEE Trans. Ind. Electron.*, vol. 70, no. 5, pp. 4875–4886, May 2023.

[15] Z. Wang and R. S. Balog, "Arc fault and flash signal analysis in DC distribution systems using wavelet transformation," *IEEE Trans. Smart Grid*, vol. 6, no. 4, pp. 1955–1963, Jul. 2015.

[16] K. Koziy, B. Gou, and J. Aslakson, "A low-cost power-quality meter with series arc-fault detection capability for smart grid," *IEEE Trans. Power Del.*, vol. 28, no. 3, pp. 1584–1591, Jul. 2013.

[17] H. Wang, X. Wang, T. Fan, J. Wang, Z. Lin, Y. Shen, J. Su, and P. Zhang, "DC series arc fault detection method in photovoltaic system based on multiple frequency selections for common-mode conductive voltage," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 15538–15553, Dec. 2022.

[18] H.-P. Park, S.-J. Chang, J.-Y. Park, M. Kim, W. Kim, and S. Chae, "DC series arc fault detection method with resonant filter design for PV systems," *IEEE Trans. Power Electron.*, vol. 39, no. 11, pp. 14240–14250, Nov. 2024.

[19] H.-P. Park and S. Chae, "DC series arc fault detection algorithm for distributed energy resources using arc fault impedance modeling," *IEEE Access*, vol. 8, pp. 179039–179046, 2020.

[20] S. Chen, X. Li, and J. Xiong, "Series arc fault identification for photovoltaic system based on time-domain and time-frequency-domain analysis," *IEEE J. Photovolt.*, vol. 7, no. 4, pp. 1105–1114, Jul. 2017.
[21] S. Hwang, B. Kim, M. Kim, and H.-P. Park, "AC series arc fault detection for wind power systems based on phase lock loop with time and frequency domain analyses," *IEEE Trans. Power Electron.*, vol. 39, no. 10, pp. 12446–12455, Oct. 2024.
[22] S. Lu, T. Sirojan, B. T. Phung, D. Zhang, and E. Ambikairajah, "DA-DCGAN: An effective methodology for DC series arc fault diagnosis in photovoltaic systems," *IEEE Access*, vol. 7, pp. 45831–45840, 2019.
[23] V. Le, C. Miller, B.-H. Tsao, and X. Yao, "Series arc fault identification in DC distribution based on random forest predicted probability," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 6, pp. 5636–5648, Dec. 2023.
[24] R. D. Telford, S. Galloway, B. Stephen, and I. Elders, "Diagnosis of series DC arc faults—A machine learning approach," *IEEE Trans. Ind. Informat.*, vol. 13, no. 4, pp. 1598–1609, Aug. 2017.
[25] Y.-L. Shen and R.-J. Wai, "Wavelet-analysis-based singular-value-decomposition algorithm for weak arc fault detection via current amplitude normalization," *IEEE Access*, vol. 9, pp. 71535–71552, 2021.
[26] Y. Mao, S. Safa, G. Smith, L. Wurth, R. Weiss, and J. Hagemeyer, "Why AI: A comparative study for detection methods in DC series arc fault," *IEEE Access*, vol. 13, pp. 42703–42722, 2025.
[27] K. C. Paul, D. Waldmann, C. Chen, Y. Wang, and T. Zhao, "Artificial intelligence for DC arc fault detection in photovoltaic systems: A comprehensive review," *IEEE Access*, vol. 13, pp. 90766–90794, 2025.
[28] X. Hu, "SMNet: A novel compositional generalization model for industrial robot multi-joint fault diagnosis," *IEEE Internet Things J.*, early access, Jan. 12, 2026, doi: 10.1109/JIOT.2026.3652582.
[29] X. Hu, H. Zhang, J. Cao, Y. Huang, X. Zhang, H. Wang, and T. Tang, "PSRONet: A deep reinforcement learning-based sensor configuration framework in railway point machines fault diagnosis," *IEEE Trans. Instrum. Meas.*, vol. 75, pp. 1–13, 2026.
[30] X. Guo, L. Wang, Y. Zhao, G. Wang, G. Liu, and Q. Zhong, "Reliability-oriented selection for grid-connected converters: A low voltage direct current microgrid case study," *IEEE Access*, vol. 8, pp. 205836–205847, 2020.
[31] M. H. Ibrahim, E. A. Badran, and M. H. Abdel-Rahman, "Detect, classify, and locate faults in DC microgrids based on support vector machines and bagged trees in the machine learning approach," *IEEE Access*, vol. 12, pp. 139199–139224, 2024.
[32] D. Cheng, B. Zhang, S. Xiong, Z. Xie, and Z. Xue, "Residual current detection prototype and simulation method in low voltage DC system," *IEEE Access*, vol. 10, pp. 51100–51109, 2022.
[33] Y. Li, J. Xu, and Z. Geng, "Accurate arc modeling of single-phase arc grounding fault in distribution network and research on dynamic arc energy," *IEEE Access*, vol. 13, pp. 110255–110267, 2025.
[34] A. D. Stokes and W. T. Oppenlander, "Electric arcs in open air," *J. Phys. D, Appl. Phys.*, vol. 24, no. 1, pp. 26–35, Jan. 1991.

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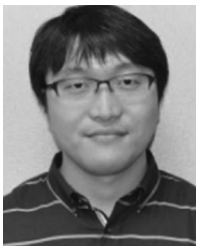

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