

Article

Effects of Carrier Trapping and Noise in Triangular-Shaped GaN Nanowire Wrap-Gate Transistor

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Abstract

The most widely used nanowire channel architecture for creating state-of-the-art high-performance transistors is the nanowire wrap-gate transistor, which offers low power consumption, high carrier mobility, large electrostatic control, and high-speed switching. The frequency-dependent capacitance and conductance measurements of triangular-shaped GaN nanowire wrap-gate transistors are measured in the frequency range of 1 kHz–1 MHz at room temperature to investigate carrier trapping effects in the core and at the surface. The performance of such a low-dimensional device is greatly influenced by its surface traps. With increasing applied frequency, the calculated trap density promptly decreases, from $1.01 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ at 1 kHz to $8.56 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at 1 MHz, respectively. The $1/f$ -noise features show that the noise spectral density rises with applied gate bias and shows $1/f$ -noise behavior in the accumulation regime. The fabricated device is controlled by $1/f$ -noise at lower frequencies and $1/f^2$ -noise at frequencies greater than ~ 0.2 kHz in the surface depletion regime. Further generation–recombination (G-R) is responsible for the $1/f^2$ -noise characteristics. This process is primarily brought on by electron trapping and detrapping via deep traps situated on the nanowire’s surface depletion regime. When the device works in the deep-subthreshold regime, the cut-off frequency for the $1/f^2$ -noise characteristics further drops to a lower frequency of 30 Hz– 10^4 Hz.

Keywords: wrap-gate transistor; nanowire; GaN; core and surface; trap effects



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1. Introduction

Planar metal-oxide semiconductor field-effect transistors (MOSFETs), based on silicon (Si), have dominated the global semiconductor market since the first integrated circuit (IC) was invented in 1958 [1,2]. They are still used to construct microelectronic devices like contemporary microprocessors, which can integrate over one billion transistors on a

single IC [3,4]. Alternative device architectures are necessary to attain better integration level and reduce power consumption in ICs as MOSFETs scaling approaches the end of Moore's law roadmap [1–4]. Devices that function as switches and regulate the flow of electricity are typically needed for power electronics. To reduce off-state leakage, a power switching device should ideally have high breakdown voltages and very little current flow in the off-state (I_{off}) [5]. To reduce conduction losses, the device should be able to have a high maximum current while maintaining low on-resistance (R_{on}) [5,6]. Over the past few decades, Si has been the preferred semiconductor material for power devices because of its abundant availability and ease of manufacturing [5,7]. However, alternative semiconductor materials are required since Si is theoretically limited as a channel material [8].

For power amplifier applications, wide-bandgap materials like gallium nitride (GaN) offer exceptional characteristics like high power operation, high frequency, and high conductivity [9–12]. High-electron-mobility transistors (HEMTs) of the AlGaN/GaN combination can function well at high breakdown voltage in the kV range [13]. The gate–drain spacing must be increased, which will result in a larger chip and greater fabrication costs, to attain a high breakdown voltage in the planar device [14]. Furthermore, surface trapping and substrate leakage limit the performance of planar devices.

Recently, nanowire FET research has expanded in response to these practical challenges [15]. Nanowire FETs are good options for next-generation nano-electronics/optoelectronics applications due to their distinct physical/chemical characteristics [16,17]. Researchers from all around the world are drawn to the nanowire wrap-gate transistor among the new alternative's topologies [18,19]. This is because of its high integrating density, excellent electrostatic control over the channel, and reduced short channel effects [20]. These days, GaN nanowire wrap-gate transistors are developed because of their high surface-to-volume ratio and enhanced electrostatic control on channel [21]. In addition, these triangular-shaped nanowire transistors have the minimum cross-sectional area under the similar line width case and hence have foremost electrostatic dominion capability and can acquire significant device performance compared to square- and circular-shaped nanowire transistors [22].

In fact, nanowire devices' electrical properties are typically restricted by carrier traps or defects that originate at the nanowire's core/surfaces. As generation–recombination (G–R) centers, carrier trap levels or deep trap levels start close to the mid-gap energy and could affect carrier transit [23,24]. Trapped charges induce fluctuations in the carrier mobility, electric field, diffusion coefficient, space charge region width, barrier height, etc. Therefore, to control the electrical properties of nanowire devices, it is critical to understand trap behavior. Understanding the effects of trapping features at the surface and/or in the core of the double-transferred GaN nanowire channels on the devices' performance in this study requires an understanding of the capacitance and conductance values based on frequency, along with the related noise characteristics. The main objective of this study is to use capacitance conductance characteristics seen in the frequency range of 1kHz to 1MHz to investigate the carrier trap characteristics at the nanowire's surface/core. The second objective is to estimate the surface trap density. Finally, the $1/f$ -noise properties of the one-dimensional GaN nanowire wrap-gate transistor are evaluated.

2. Materials and Methods

Soitec's Smart CutTM technology was used to fabricate the GaN on insulator (GaNOI) structure using dual-wafer-transfer procedures [24]. A GaN film layer (150 nm) and oxide layer (800 nm) were positioned on a sapphire (Al_2O_3) substrate to form the 4-inch GaNOI wafer structure. The triangular-shaped GaN nanowire transistor fabrication procedure was as follows (Figure 1). Using polymethyl methacrylate (PMMA) solution on the surface

of the GaNOI wafer structure, electron-beam (E-beam) lithography was employed to form a pattern along the $\langle 11\bar{2}0 \rangle$ direction to define the initial active region (Figure 1a). TMAH solution was applied to the patterned GaN stripe for 10 min at 90 °C to avoid plasma damage and minimize surface roughness. Due to the strong anisotropic chemical nature of the TMAH solution, it etches in the lateral direction without causing any vertical etching direction $\langle 0001 \rangle$ (Figure 1b). A triangular-shaped one-dimensional GaN nanowire with a height of approximately 56 nm and sloped sidewall surfaces corresponding to $\langle 1\bar{1}00 \rangle$ occurred by using the tetramethylammonium hydroxide (TMAH) solution along the $\langle 1\bar{1}01 \rangle$ direction, which decreased the stripe width. To fully remove the oxide beneath the one-dimensional GaN nanowire, the wafer must be dipped in a buffered oxide etch (BOE) solution (Figure 1c).

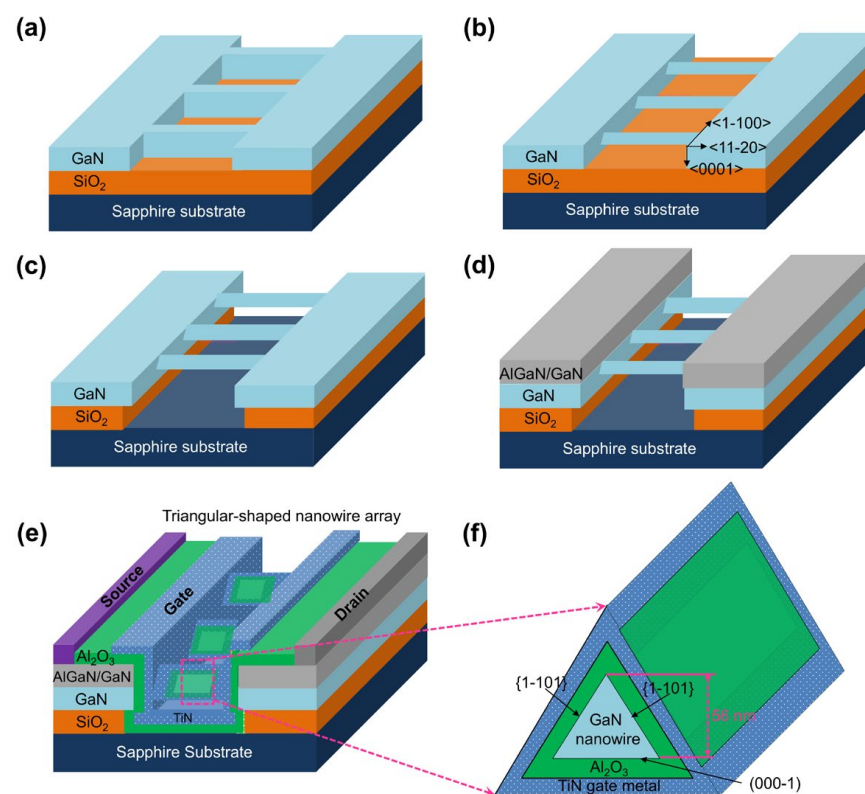


Figure 1. Fabrication process for triangular-shaped GaN nanowire wrap-gate transistor: (a) the separation of GaN nanowires; (b) reduction of GaN nanowire arrays by chemical etchant along $\{1\bar{1}01\}$ direction, resulting in triangular-shaped nanowire; (c) separation of triangular-shaped GaN nanowire arrays by etching the SiO₂ layer; (d) deposition of AlGaIn/GaN layer on the patterned surface; (e) schematic illustration of triangular-shaped GaN transistor; (f) a cross-section diagram of the triangular-shaped GaN nanowire.

MOCVD was used to deposit an undoped GaN film (50 nm) and an Al_{0.3}Ga_{0.7}N film (20 nm) in certain regions on the patterned GaN wafer surface (Figure 1d). The r -plane on the patterned GaN wafer surface experiences a self-limiting growth process along its $\{1\bar{1}01\}$ direction. N atoms on the surfaces of the r -plane simply interacted with H atoms to create N–H bonds during the MOCVD growth process, stabilizing the plane and limiting the growth. Because of the $\{1\bar{1}01\}$ crystal direction, the AlGaIn/GaN films were therefore only successfully deposited in the source/drain (S/D) regimes and not on the surface of GaN nanowires; as a result, the one-dimensional GaN nanowire's area remained unchanged. Regrowing AlGaIn/GaN films in the source/drain area has the benefit of depositing a two-dimensional electron gas (2DEG), which lowers the device's series resistance.

Next, utilizing plasma-enhanced chemical vapor deposition (PECVD) technology, Al_2O_3 (20 nm) and TiN (10 nm) films were chosen as an insulating gate material and for the metal-gate electrode, respectively, and deposited sequentially. Ti/Al/Ni/Au metal layers were then deposited using the E-beam deposition method after contact holes were unlatched to connect the S/D regions. The resultant metal layers were annealed using a rapid thermal process (RTP) system for 30 s in N_2 -gas flow. A high-resolution transmission electron microscope (HRTEM, JEOL, JEM-2100F, Tokyo, Japan) was used to analyze the device cross-section. Using a semiconductor source meter unit (B1500A, Agilent, Santa Clara, CA, USA), the current, capacitance, and conductance values of the one-dimensional GaN nanowire wrap-gate transistor were measured. Here, the B1500A semiconductor parameter analyzer can be used to characterize capacitance and conductance by employing its impedance measurement unit (IMU). The IMU applies a small AC signal at various frequencies to the device under test (DUT) and measures the resulting current. By analyzing the amplitude and phase relationship between the voltage and current, the B1500A can determine the capacitance and conductance of the DUT at each frequency. A completely automated noise measurement system (NOISYS7, Synergie Concept/Instrumentation & Electronic, Meylan, France) was used to measure the $1/f$ -noise.

3. Results

The schematic device structure of the studied GaN nanowire wrap-gate transistor is shown in Figure 2a, which contains 64 one-dimensional GaN nanowires in the shape of triangles, each having two identical crystal faces $\{1\bar{1}01\}$. A bright-field HR-TEM image on the right side of Figure 2b makes it evident that the AlGaIn/GaN nanowire core is triangular-shaped and surround by gate oxides (Al_2O_3) and gate metal (TiN). The triangular-shaped wrap-gate GaN nanowire transistor normally operates off with a threshold voltage (V_{th}) of approximately 3.5 V, as seen in Figure 3. This high value is potentially achieved because of the fully depleted triangular-shaped wrap-gate GaN nanowire. At $V_{\text{gs}} = 7$ V and $V_{\text{ds}} = 0.1$ V, the highest transconductance (g_m) peak is around $0.94 \mu\text{S}$, while the maximum drain current ($I_{\text{ds,max}}$) is approximately $4.1 \mu\text{A}$. Additionally, Figure 4 shows the semi-logarithmic transfer characteristics. The leakage current of the triangular-shaped wrap-gate GaN nanowire transistor is as low as around 10^{-13} A/mm. The $I_{\text{on}}/I_{\text{off}}$ ratio of 10^7 is high for the triangular-shaped wrap-gate GaN nanowire transistor. Further, the field-effect carrier mobility of the double-transferred wrap-gate GaN nanowire transistor is $15 \text{ cm}^2/\text{V}\cdot\text{s}$. Furthermore, the subthreshold swing of the fabricated device is 130 mV/decade.

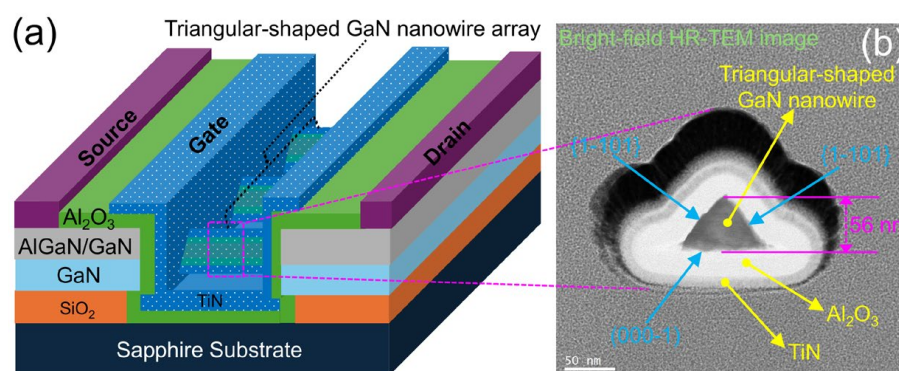


Figure 2. (a) The triangular-shaped GaN nanowire wrap-gate transistor's schematic diagram. (b) A bright-field high-resolution transmission electron microscopy cross-sectional picture.

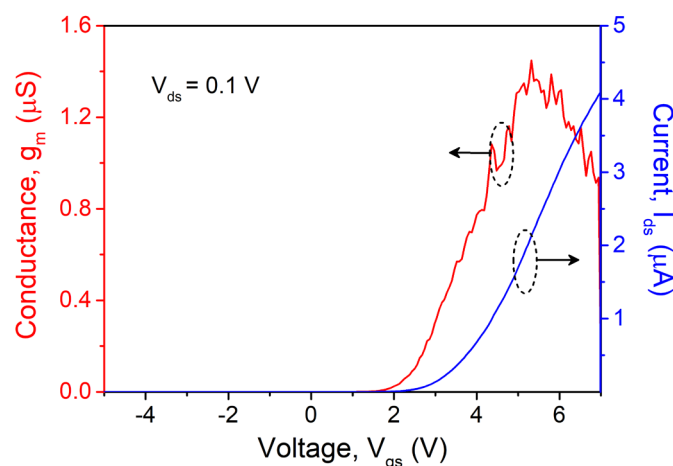


Figure 3. Linear data plots of the drain current (I_{ds}) (i.e., right-side) and transconductance (g_m) (i.e., left-side) vs. gate-source voltage (V_{gs}) at applied drain voltage of $V_{ds} = 0.1$ V.

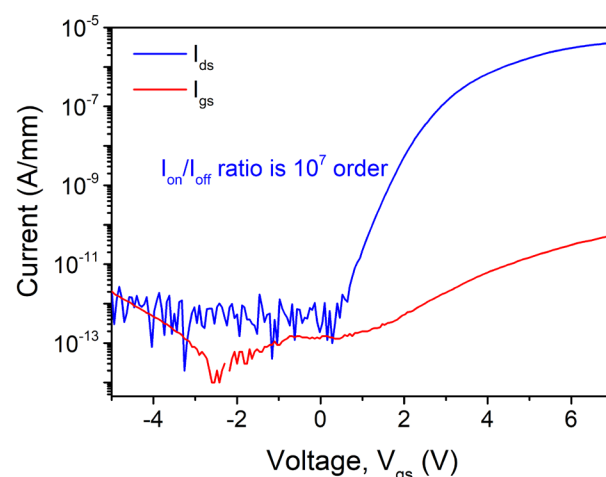


Figure 4. Data plots of I_{ds} and I_{gs} vs. V_{gs} at applied drain voltage of $V_{ds} = 0.1$ V.

Three distinct voltage-dependent regimes are seen in the frequency-dependent capacitance characteristics of the triangular-shaped wrap-gate GaN nanowire transistor measured at the comparatively low frequency of 1 kHz, as shown in Figure 5: accumulation, surface depleted and fully depleted regimes of the whole GaN nanowire channel. Because of the very long lifetime in the case of GaN-related materials, the surface inversion at $V_{gs} < 0$ V has been eliminated [24,25]. As the frequency increases, it is observed that the triangular-shaped wrap-gate GaN nanowire transistor shows a significant positive shift in flat-band voltage (V_{FB}) with grievous frequency dispersion. There is also a distinguishable hysteresis of the shift in V_{FB} (i.e., ΔV_{FB}) between the bias sweeps, but the ΔV_{FB} falls with rising frequency. The existence of many surface traps with different lifetimes is reflected in this extreme frequency dispersion. A substantial interface trap capacitance (C_{it}) is associated with this; the traps respond effectively to low and intermediate frequencies of alternating current (AC) signals, but they barely react at high frequencies [26,27]. The frequency scattering may also be brought about by the deep-level traps that were added to the GaN nanowire during the previously mentioned dual-wafer-transfer process. A severe dispersion in the accumulation regime and a positive shift in V_{FB} with increasing frequency result from the trapped carriers' inability to respond to the AC signal at high frequencies, which prevents them from contributing to the current movement and drastically lowers the determined capacitance [24,28].

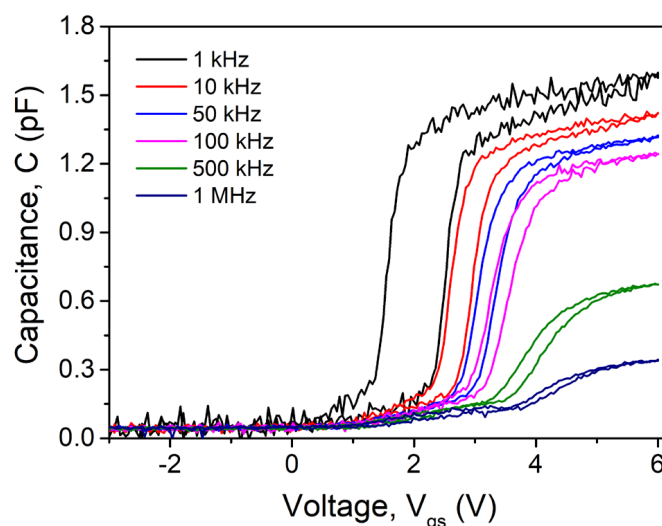


Figure 5. Frequency-dependent capacitance (C) vs. gate-source voltage (V_{gs}) of the measured transistor.

The frequency-dependent conductance characteristics are displayed in Figure 6. In opposition to the capacitance properties, the conductance plots shift to negative bias, and the conductance rises with rising frequency. Additionally, it is observed that a conductance peak develops at low frequencies (less than 100 kHz) but vanishes at higher frequencies (500 kHz and 1 MHz) when $V_{gs} < V_{th}$. The presence of surface traps with different time responses, as mentioned in the capacitance measurement, is the exact same source of conductance behavior. This indicates that the traps may readily follow the AC wave signal at low frequencies (the value of the period is greater than the carrier lifetime of charge in the traps), which subsequently clearly contributes to the conductance of the device [29,30]. In comparison with low frequencies (> 500 kHz), the traps are nearly impossible to follow at high frequencies and do not contribute to the observed conductance. The charges in surface-level traps cannot ensure the AC wave signal at prominent frequencies because the time constant is significantly greater than the period, unlike at low frequencies.

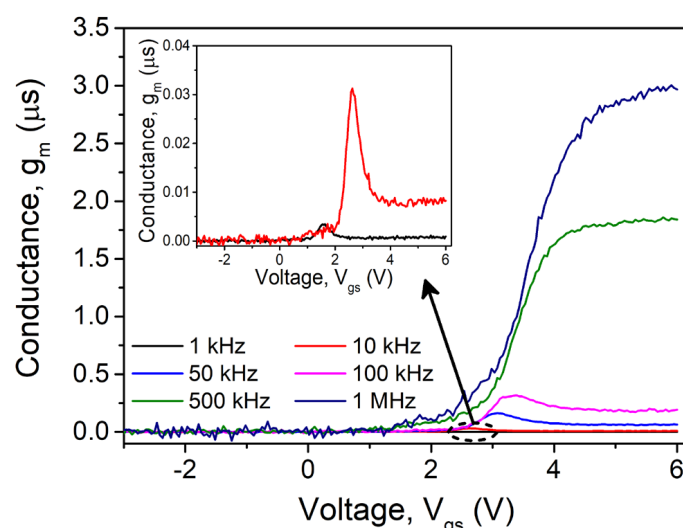


Figure 6. Frequency-dependent conductance (g_m) vs. gate-source voltage (V_{gs}) of measured transistor.

Using capacitance and conductance values, the Hill–Coleman technique is used to assess the frequency-dependent interface trap density (D_{it}) values [31]. The following technique can be used to determine the D_{it} values:

$$D_{it} = \frac{2}{qA} \left(\frac{(g_m/\omega)_{max}}{((g_m/\omega)_{max} C_{OX})^2 + (1 - C/C_{OX})^2} \right) \quad (1)$$

where q , A , and C_{OX} are charge, area of contact, and oxide capacitance (i.e., determined from capacitance/conductance measurements in strong accumulation regime at maximum applied frequency range (1 MHz)). As Figure 7 illustrates, the extracted D_{it} values gradually drop with increasing frequency. Additionally, it is seen that the D_{it} values derived from Equation (1) are comparable to those derived from the typical low-frequency oxide/nitride-semiconductor contacts. The significant dispersion effects on the capacitance and conductance properties are caused by the high value of D_{it} . Here, D_{it} deactivation with increasing frequency can account for the rise in V_{FB} and fall in ΔV_{FB} with rising frequency, as illustrated in Figures 5 and 6.

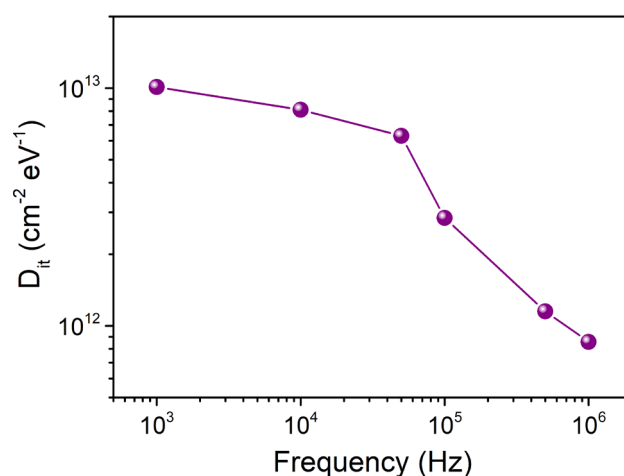


Figure 7. Plot of frequency-dependent interface trap density (D_{it}).

Next, measurements of low-frequency noise are taken to better examine the trapping effect in the triangular-shaped wrap-gate GaN nanowire transistor. It is commonly known that $1/f$ -noise measurements can give accurate data on the nature of carrier conduction in bulk materials and at the surface when combined with other electrical characteristics. The $1/f$ -noise measurements are employed to assess the quality of semiconductor devices and investigate impurity and deep-level traps in crystalline semiconductors [32,33]. In the frequency range of 4– 10^4 Hz at $V_{ds} = 0.1$ V, the noise spectral density (S_{Id}) of the voltage deviations varied regarding frequency. The bias varied from the deep-subthreshold regime to strong accumulation. The S_{Id} increases with gate voltage, as seen in Figure 8a. As previously mentioned in the capacitance and conductance measurements, the noise is primarily caused by the carrier transport between the shallow states and the accumulation channel; as evidenced by the noise curves, there is an obvious $1/f$ shape in all measured frequency regimes in the extreme accumulation regime ($V_{gs} > V_{th} = 3.5$ V).

However, the noise spectra in the depletion regime ($2.4 \text{ V} < V_{gs} < V_{th}$) take on a $1/f$ shape at lower frequencies and change to a $1/f^2$ shape at frequencies greater than about 0.2 kHz. The G–R noise resulting from the carrier transport mechanism via deep-level traps, which have a longer time constant but a comparatively shorter one than the surface traps, is responsible for these $1/f^2$ curves. This indicates that the carriers undergo both surface and surface depletion regime trapping and detrapping in the GaN nanowire channel. The cut-off frequency (f_c) for the $1/f^2$ curves moves to lower frequencies of 30 Hz– 10^4 Hz in the deep-subthreshold regime ($V_{gs} < 2.4$ V).

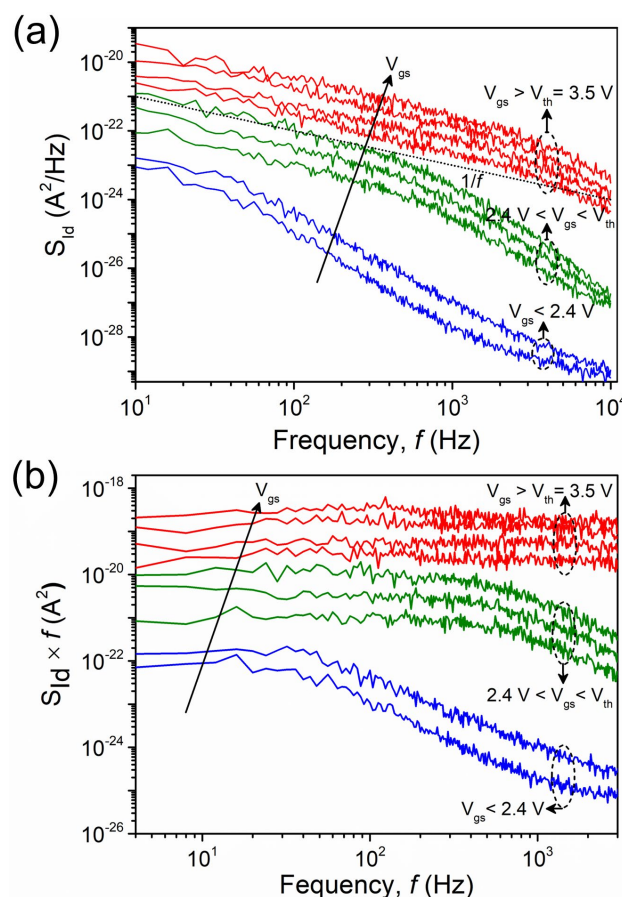


Figure 8. (a) Noise spectral density (S_{Id}) and (b) $S_{Id} \times f$ values according to the frequency of the fabricated transistor at $V_{ds} = 0.1$ V.

The graph for the S_{Id} multiplied by the frequency versus frequency in Figure 8b clearly shows the $1/f^2$ shape. From the cut-off frequency for the $1/f^2$ curves, we can extract the time constant (τ_i) using the following equation:

$$S_{Id} \times f = K_f + \sum_{i=0}^N \frac{A_i f}{1 + \left(\frac{f}{f_c}\right)^2}, \quad \tau_i = \frac{1}{2\pi f_c} \quad (2)$$

where K_f is the flicker noise coefficient of the $1/f$ noise and A_i is the Lorentzian plateau value of G–R noise component. The calculated τ_i are 3.2 ms and 0.5 ms for the deep-subthreshold regime ($V_{gs} < 2.4$ V) in the surface depletion regime ($2.4 \text{ V} < V_{gs} < V_{th}$), respectively. In fact, the fully depleted GaN nanowire channel is dominated by the G–R-related carrier transport mechanism, which includes comparatively longer time constants [34,35]. The deep-level traps' influence on capacitance and conductance values is consistent with their role in the noise characteristics.

4. Conclusions

Frequency-dependent capacitance and conductance values were used to examine the trapping effects and noise properties of a triangular-shaped wrap-gate GaN nanowire transistor that was created using a dual-transfer and top-down method. It was discovered that the capacitance, conductance, and noise properties are significantly influenced by the high trap density at the triangular-shaped GaN nanowire channel's surface and core. The results can be described as follows: (i) The carrier conduction between the accumulation surface channel and the shallow traps is efficient in the accumulation area ($V_{gs} < V_{th} = 3.5$ V), ex-

hibiting $1/f$ -noise behavior with applied gate biases. (ii) The carrier transport mechanism via the deep-level traps in the triangular-shaped GaN nanowire channel's depletion regime ($2.4 \text{ V} < V_{\text{gs}} < V_{\text{th}}$) becomes effective in the surface depletion regime, resulting in G–R noise with $1/f^2$ plot at frequencies higher than $\sim 5 \text{ kHz}$ rather than $1/f$ shape at lower frequencies. (iii) In the deep-subthreshold regime ($V_{\text{gs}} < 2.4 \text{ V}$), the G–R-based carrier transport mechanism prevails via the deep-level traps in the fully and deeply depleted triangular-shaped GaN nanowire channel, resulting in a reduction in cut-off frequency for $1/f^2$ noise to a lower range of $30 \text{ Hz} \sim 10^4 \text{ Hz}$. The evolution of high-efficiency GaN-based nanowire transistor for upcoming nano-level electronic devices requires an understanding of trap characteristics which these results help to provide.

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Data Availability Statement: The data are available on reasonable request from the corresponding author.

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References

1. Salahuddin, S.; Ni, K.; Datta, S. The era of hyper-scaling in electronics. *Nat. Electron.* **2018**, *1*, 442–450. [\[CrossRef\]](#)
2. Wang, X.; Liu, C.; Wei, Y.; Feng, S.; Sun, D.; Chen, H. Three-dimensional transistors and integration based on low-dimensional materials for the post-Moore's law era. *Mater. Today* **2023**, *63*, 172–187. [\[CrossRef\]](#)
3. Chau, R.; Doyle, B.; Datta, S.; Kavalieros, J.; Zhang, K. Integrated nanoelectronics for the future. *Nat. Mater.* **2007**, *6*, 810–812. [\[CrossRef\]](#)
4. Fatahilah, M.F.; Yu, F.; Stempel, K.; Romer, F.; Maradan, D.; Meneghini, M.; Baki, A.; Hohls, F.; Schumacher, H.W.; Witzigmann, B.; et al. Top-down GaN nanowire transistors with nearly zero gate hysteresis for parallel vertical electronics. *Sci. Rep.* **2019**, *9*, 10301. [\[CrossRef\]](#) [\[PubMed\]](#)
5. Ruzzarin, M.; Santi, C.D.; Yu, F.; Fatahilah, M.F.; Stempel, K.; Waisto, H.S.; Waag, A.; Meneghesso, G.; Zanoni, E.; Meneghini, M. Highly stable threshold voltage in GaN nanowire FETs: The advantages of p-GaN channel/Al₂O₃ gate insulator. *Appl. Phys. Lett.* **2020**, *117*, 203501. [\[CrossRef\]](#)
6. Lorenz, L.; Mauder, A. *Technology Guide: Principles—Applications—Trends*; Springer: Berlin/Heidelberg, Germany, 2009; p. 78.
7. Millan, J.; Godignon, P.; Perpina, X.; Perex-Tomas, A.; Rebollo, J. A survey of wide bandgap power semiconductor device. *IEEE Trans. Power Electron.* **2014**, *29*, 2155–2163. [\[CrossRef\]](#)
8. Hu, J.; Zhang, Y.; Sun, M.; Piedra, D.; Chowdhury, N.; Palacios, T. Materials and processing issues in vertical GaN power electronics. *Mater. Sci. Semicond. Process* **2018**, *78*, 75–84. [\[CrossRef\]](#)
9. Yuvaraja, S.; Khandelwal, V.; Tang, X.; Li, X. Wide bandgap semiconductor-based integrated circuits. *Chip* **2023**, *2*, 100072. [\[CrossRef\]](#)
10. Lu, H.; Zhang, M.; Yang, L.; Hou, B.; Martinez, R.P.; Mi, M.; Du, J.; Deng, L.; Wu, M.; Chowdhury, S.; et al. A review of GaN RF devices and power amplifiers for 5G communication applications. *Fundam. Res.* **2025**, *5*, 315–331. [\[CrossRef\]](#)
11. Murugan, C.A.; Murugapandian, P.; Sivamani, C.; Haripriya, D. Advancing the frontiers of N-polar GaN HEMT technology: Materials, architectures, and applications in RF and power electronics. *Mater. Sci. Semicond. Process* **2025**, *199*, 109874. [\[CrossRef\]](#)
12. Fan, K.; Guo, J.; Huang, Z.; Xu, Y.; Huang, Z.; Xu, W.; Wang, Q.; Lin, Q.; Li, X.; Liu, H.; et al. GaN-on-diamond technology for next generation power devices. *Moore. More* **2025**, *2*, 8. [\[CrossRef\]](#)

13. Herbecq, N.; Roch-Jeune, I.; Linge, A.; Grimbert, B.; Zegaoui, M.; Medidoub, F. GaN-on-silicon high electron mobility transistors with blocking voltage of 3 kV. *Electron. Lett.* **2015**, *51*, 1532–1534. [[CrossRef](#)]
14. Tian, Z.; Ji, X.; Yang, D.; Liu, P. Research progress in breakdown enhancement for GaN-based high electron-mobility transistors. *Electronics* **2023**, *12*, 4435. [[CrossRef](#)]
15. Wu, Y.H.; Kim, H.H.; Shin, J.C. Improved mobility in InAs nanowire FETs with sulfur-based surface treatment. *Curr. Appl. Phys.* **2025**, *70*, 81–86. [[CrossRef](#)]
16. Arjmand, T.; Legallais, M.; Nguyen, T.T.T.; Serre, P.; Vallejo-Perez, M.; Morisot, F.; Salem, B.; Ternon, C. Functional devices from bottom-up silicon nanowires: A review. *Nanomaterials* **2022**, *12*, 1043. [[CrossRef](#)]
17. Salhi, B.; Hossain, M.K.; Mukhaimer, A.W.; Al-Sulaiman, F.A. Nanowires: A new pathway to nanotechnology-based applications. *J. Electroceram.* **2016**, *37*, 34–49. [[CrossRef](#)]
18. Mallem, S.P.R.; Im, K.-S.; Thingujam, T.; Lee, J.-H.; Caulmilone, R.; Cristoloveanu, S. Gate architecture effects on the gate leakage characteristics of GaN wrap-gate nanowire transistors. *Electron. Mater. Lett.* **2020**, *16*, 433–440. [[CrossRef](#)]
19. Mallem, S.P.R.; Puneetha, P.; Choi, Y.; Baek, S.M.; Lee, D.Y.; Im, K.-S.; An, S.J. Barrier height, ideality factor and role of inhomogeneities at the AlGaIn/GaN interface in GaN nanowire wrap-gate transistor. *Nanomaterials* **2023**, *13*, 3159. [[CrossRef](#)]
20. Singh, S.; Dhar, R.S.; Banerjee, A.; Gupta, V. Design and analysis of high-K wrapped GaN gate all around FET as high-frequency device in IOT systems. *IEEE Access* **2025**, *13*, 78833. [[CrossRef](#)]
21. Mallem, S.P.R.; Puneetha, P.; Lee, D.Y.; Kim, Y.; Kim, H.J.; Im, K.-S.; An, S.J. Carrier trap and their effects on the surface and core of AlGaIn/GaN nanowire wrap-gate transistor. *Nanomaterials* **2023**, *13*, 2132. [[CrossRef](#)]
22. Li, M.; Chen, G.; Huang, R. High performance GAA SNWT with a triangular cross section: Simulation and experiments. *Appl. Sci.* **2018**, *8*, 1553. [[CrossRef](#)]
23. Narita, T.; Ito, K.; Iguchi, H.; Kikuta, D.; Kanechika, M.; Tomita, K.; Iwasaki, S.; Kataoka, K.; Kano, E.; Ikarashi, N. Engineered interface charges and traps in GaN MOSFETs providing high channel mobility and E-mode operation. *Jpn. J. Appl. Phys.* **2024**, *63*, 120801. [[CrossRef](#)]
24. Reddy, M.S.P.; Im, K.-S.; Lee, J.-H.; Caulimione, R.; Cristoloveanu, S. Trap and 1/f-noise effects at the surface and core of GaN nanowire gate-all-around FET structure. *Nano Res.* **2019**, *12*, 809–814. [[CrossRef](#)]
25. Kang, H.S.; Reddy, M.S.P.; Kim, D.S.; Kim, K.W.; Ha, J.B.; Lee, Y.S.; Choi, H.C.; Lee, J.H. Effect of oxygen species on the positive flat-band voltage shift in Al₂O₃/GaN metal-insulator-semiconductor capacitors with post-deposition annealing. *J. Phys. D Appl. Phys.* **2013**, *46*, 155101. [[CrossRef](#)]
26. Matys, M.; Adamowich, B.; Domanowska, A.; Michalewicz, A.; Stoklas, R.; Akazawa, M.; Yatabe, Z.; Hashizume, T. On the origin of interface states at oxide/III-nitride heterojunction interfaces. *J. Appl. Phys.* **2016**, *120*, 225305. [[CrossRef](#)]
27. Bülbül, M.M.; Zeyrek, S. Frequency dependent capacitance and conductance—Voltage characteristics of Al/Si₃N₄/p-Si (100) MIS diodes. *Microelectron. Eng.* **2006**, *83*, 2522–2526. [[CrossRef](#)]
28. Taoka, N.; Kubo, T.; Yamada, T.; Egawa, T.; Shimizu, M. Understanding of frequency dispersion in C–V curves of metal-oxide-semiconductor capacitor with wide-bandgap semiconductor. *Microelectron. Eng.* **2017**, *178*, 182–185. [[CrossRef](#)]
29. Güçlü, Ç.Ş.; Özdemir, A.F.; Kökce, A.; Altındal, Ş. Frequency and voltage-dependent dielectric properties and AC electrical conductivity of (Au/Ti)/Al₂O₃/n-GaAs with thin Al₂O₃ interfacial layer at room temperature. *Acta Phys. Pol. A* **2016**, *130*, 325–330. [[CrossRef](#)]
30. Nicollian, E.H.; Brews, J.R. *MOS (Metal-Oxide-Semiconductor) Physics and Technology*; John Wiley & Sons: New York, NY, USA, 1982.
31. Hill, W.A.; Coleman, C.C. A single-frequency approximation for interface state density determination. *Solid State Electron.* **1980**, *23*, 987–993. [[CrossRef](#)]
32. Balandin, A.; Cai, S.; Li, R.; Wang, K.L.; Rao, V.R.; Viswanathan, C.R. Flicker noise in GaN/Al_{0.15}Ga_{0.85}N doped channel heterostructure field effect transistors. *IEEE Electron Device Lett.* **1998**, *19*, 475–477. [[CrossRef](#)]
33. Levinshtein, M.E.; Rumyantsev, S.L.; Gaska, R.; Yang, J.W.; Shur, M.S. AlGaIn/GaN high electron mobility field effect transistors with low 1/f noise. *Appl. Phys. Lett.* **1998**, *73*, 1089–1091. [[CrossRef](#)]
34. Theodorou, C.G.; Fasarakis, N.; Hoffman, T.; Chiarella, T.; Ghibaud, G.; Dimitriadis, C.A. Origin of the low-frequency noise in n-channel FinFETs. *Solid State Electron.* **2013**, *82*, 21–24. [[CrossRef](#)]
35. Theodorou, C.G.; Ioannidis, E.G.; Andrieu, F.; Poiroux, T.; Faynot, O.; Dimitriadis, C.A.; Ghibaud, G. Low-frequency noise sources in advanced UTBB FD-SOI MOSFETs. *IEEE Trans. Electron. Devices* **2014**, *61*, 1161–1167. [[CrossRef](#)]

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