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ORIGINAL ARTICLE

Improved Switching Characteristics of 1.2 kV P-Shielded Split Gate SiC MOSFETs

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Abstract

1.2 kV P-shielded Split Gate SiC MOSFETs (PSG-MOSFETs) were designed to achieve a reduced reverse transfer capacitance (C_{rss}) and to effectively suppress electric field crowding at the gate oxide. The formation of the P-shielding region of PSG-MOSFETs was achieved without the necessity of an additional photo mask. The effect of the maximum electric field at the gate oxide ($E_{ox,max}$) and specific on-resistance ($R_{on,sp}$) by the P-shielding region was investigated by varying the width of the P-shielding region (W_P). As the W_P increases, the $E_{ox,max}$ is reduced due to the suppression of the electric field at the gate oxide. Conversely, the $R_{on,sp}$ increases due to the narrower current path in the JFET region. Furthermore, a comparative analysis of the simulated C_{rss} and gate-drain charge was conducted, and the reduced total switching energy losses (E_{total}) of PSG-MOSFETs were verified via the simulation of a double pulse test. The PSG-MOSFET exhibited lower $E_{ox,max}$, C_{rss}, and E_{total} in comparison to the Split Gate SiC MOSFET.

Keywords SiC · MOSFET · Split gate · Electric field crowding · Switching loss

1 Introduction

Silicon Carbide (SiC) has superior properties, including a higher critical electric field, a wider bandgap, and a higher thermal conductivity than Silicon [1–3]. These properties identify SiC as a next-generation power semiconductor [4–7]. SiC-based power devices with excellent thermal conductivity and low specific thermal resistance ($R_{on,sp}$) are key components in inverters and DC-DC converters for electric vehicles. [8–11]. For SiC MOSFETs, a reduction in the capacitances is necessary due to the significant portion of the power dissipation occurring during the switching operations [12–14]. Specifically, the reverse transfer capacitance (C_{rss}) and gate-drain charge (Q_{GD}) are the dominant parameters inducing switching losses [14–16]. Because during the charging of the C_{rss}, a simultaneous application of high voltage and current occurs [16–19]. The overlap between the poly-Si gate and JFET region is a parasitic capacitance induced by the overlap of the poly-Si gate and the JFET region.

The improved C_{rss} and Q_{GD} of Split Gate SiC MOSFETs (SG-MOSFETs) have been proposed and demonstrated [22–28]. The split gate structure can reduce the overlap area between the poly-Si gate and JFET region. This approach can result in a reduction in the gate oxide capacitance (C_{ox}) [22, 27]. However, the electric field crowding occurs at the exposed edge of the poly-Si gate of SG-MOSFETs, which could eventually result in significant damage to the gate oxide [25–28].

Several approaches for suppression of the electric field at the gate oxide of SG-MOSFETs have been reported [26–34]. The addition of a P-type layer at the bottom of the P-base in SG-MOSFETs achieves a significant decrease in the maximum electric field in gate oxide ($E_{ox,max}$) [26–28]. However, an increase in the $R_{on,sp}$ and the cell-pitch, as well as the necessity for additional photo masks, is observed [30]. Additionally, the implementation of a deep P-well structure by channeled ion implantation effectively reduce the $E_{ox,max}$ of SG-MOSFETs, without the additional photo mask [32–34].

In this paper, we proposed 1.2 kV P-shielded Split Gate SiC MOSFETs (PSG-MOSFETs). PSG-MOSFETs feature

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a P-shielding region within the JFET region, which serves to suppress the electric field crowding at the gate oxide and reduce switching losses. The P-shielding region induces the expansion of a depletion region within the JFET region, protecting the gate oxide from the electric field. Furthermore, the wide depletion region induced by the P-shielding region serves to significantly reduce the depletion capacitance (C_{dep}).

2 Device Structures and Simulation Methods

Sentaurus TCAD simulations were employed to design and analyze 1.2 kV SiC MOSFETs. All simulations are based on half-cell size and conducted with the same device area. Figure 1a–c show the 2-D cross-sectional views of the 1.2 kV SiC conventional MOSFET (C-MOSFET), SG-MOSFET, and PSG-MOSFET, respectively. A SiC N-drift region with a background doping concentration of 8×10^{15} cm^{-3} and a thickness of 10 µm on a SiC N^+ substrate was employed. The JFET region was designed with a doping concentration of 3×10^{16} cm^{-3}, a width (W_{JFET}) of 1.5 µm, and a depth of 0.8 µm to reduce the resistance of the JFET region. All structures were designed with an identical channel length of 0.5 µm and thickness of the gate oxide of 50 nm. The SG-MOSFET and PSG-MOSFET were designed with an identical length of the overlap region (L_{PJ}) of 0.3 µm between the poly-Si gate and JFET region.

Figure 2 shows the flows of process simulation for the PSG-MOSFET. The PSG-MOSFET were employed with identical process simulation flows as the C-MOSFET and SG-MOSFET. The formation of the P-shielding region within the JFET region was achieved via the employment of the ion implantation process for the P-source, without the necessity for an additional photo mask [35, 36]. The P-shielding region was designed with a depth of 0.5 µm and a width (W_P) ranging from 0.1 µm to 0.4 µm. Furthermore, it

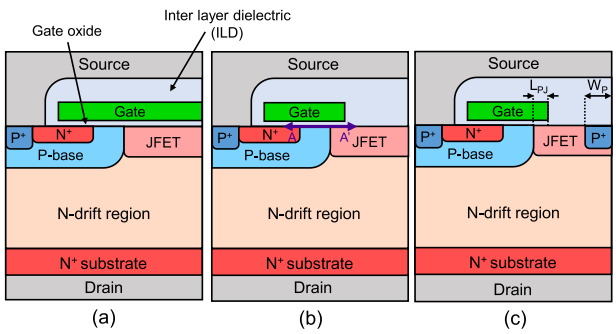

Fig. 1 2-D cross-sectional views of the **a** C-MOSFET, **b** SG-MOSFET, and **c** PSG-MOSFET

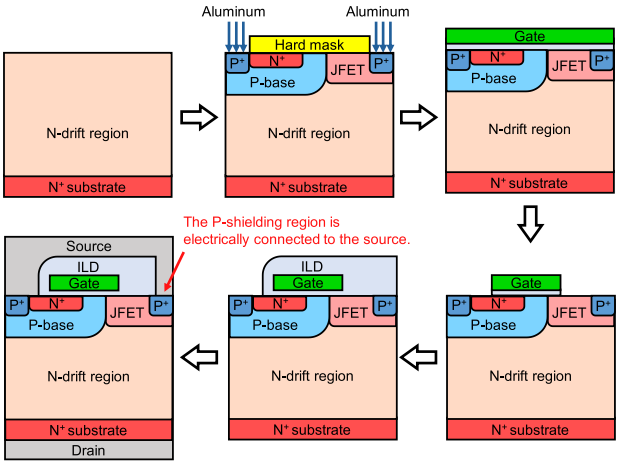

Fig. 2 Process simulation flow for the PSG-MOSFET

is noted that the P-shielding region is electrically connected to the source, which effectively improves electrical characteristics of PSG-MOSFETs [37]. Table 1 lists all device parameters used in TCAD simulation.

The Shockley–Read–Hall recombination model, the Auger recombination model, the Okuto-Crowell avalanche model, and the incomplete ionization model were employed to enhance the accuracy of the TCAD simulation. The breakdown voltage (BV) was set to a drain-source voltage (V_{DS}) when the maximum electric field in SiC ($E_{SiC,max}$) or $E_{ox,max}$ exceeded 3 MV/cm or 5 MV/cm, respectively [38].

3 Results and Discussion

Figure 3 shows the electric field distribution of the SG-MOSFET and PSG-MOSFET ($W_P = 0.3$ µm) in blocking mode with a gate-source voltage (V_{GS}) of 0 V and a V_{DS} of 1.2 kV. The SG-MOSFET exhibits an $E_{ox,max}$ of 4.78 MV/cm due to electric field crowding at the gate oxide, as shown in Fig. 3a. However, the PSG-MOSFET exhibits an $E_{ox,max}$ of 2.95 MV/cm, which is 38.28% lower than that of the SG-MOSFET, as shown in Fig. 3b. The reduced $E_{ox,max}$ of the PSG-MOSFET is due to the dispersion of the electric field from the gate oxide into the P-shielding region, which results in an $E_{SiC,max}$ of 2.32 MV/cm. Furthermore, the PSG-MOSFET exhibits a BV of 1710 V, which is 110.85% higher than that of the SG-MOSFET. It is demonstrated that the expansion of the depletion region by the P-shielding region serves to protect the gate oxide from the electric field.

To verify the enhanced blocking capability of the PSG-MOSFET, the electro-static potential at the surface of the channel region of the SG-MOSFET and the PSG-MOSFET ($W_P = 0.3$ µm) was extracted and compared, as shown in Fig. 4. As shown in Fig. 1b, the A-A' line represents the

Table 1 Device parameters used in TCAD simulation

Parameters [unit]	Value
Channel length [μm]	0.5
Thickness of the gate oxide [nm]	50
Half-cell pitch [μm]	3.4
Width of the JFET region (W_{JFET}) [μm]	1.5
Depth of the JFET region [μm]	0.8
Thickness of the N-drift region [μm]	10
Length of the overlap region between the poly-Si gate and JFET region (L_{PJ}) [μm]	0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6
Width of the P-shielding region (W_P) [μm]	0.1, 0.2, 0.3, 0.4
Depth of the P-base [μm]	1.0
Doping concentration of the N-drift region [cm^{-3}]	8×10^{15}
Doping concentration of the JFET region [cm^{-3}]	3×10^{16}
Doping concentration of the P-shielding region [cm^{-3}]	1.2×10^{20}

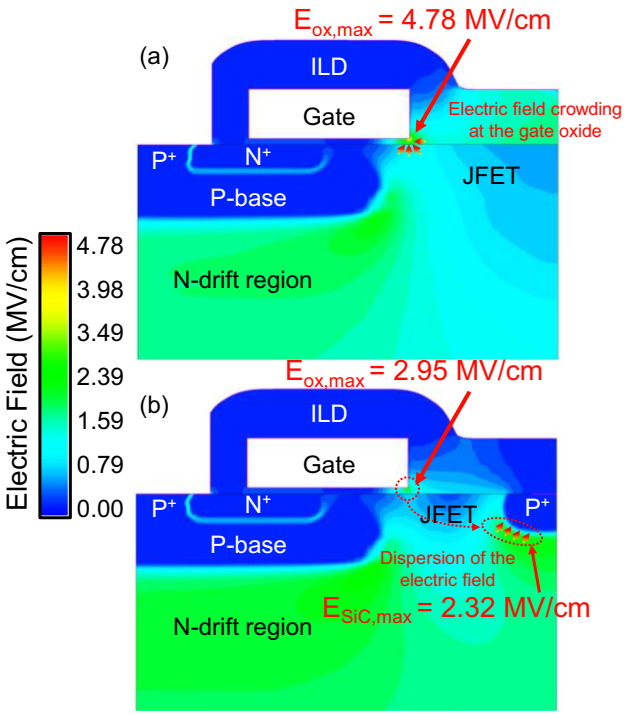

Fig. 3 Electric field distribution in blocking mode (at a V_{DS} of 1.2 kV and a V_{GS} of 0 V) for the **a** SG-MOSFET and **b** PSG-MOSFET

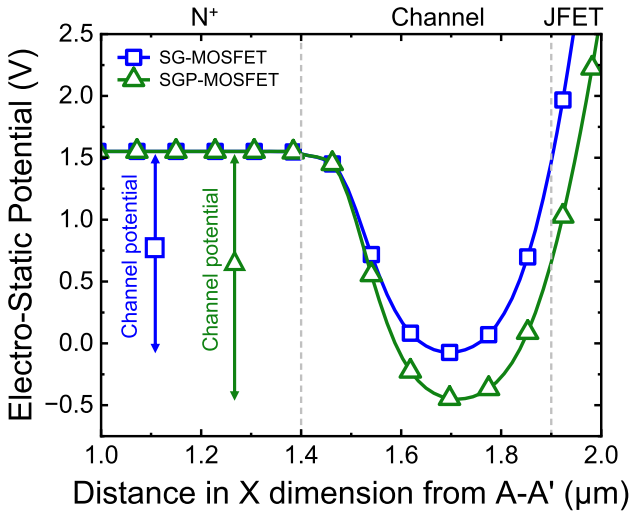

Fig. 4 Electro-static potential at the surface of the channel region in blocking mode for the SG-MOSFET and PSG-MOSFET as a function of the distance in X dimension from A-A'

surface of the channel region of the device. It is shown that the PSG-MOSFET exhibits a higher potential barrier at the channel region (channel potential) than that of the SG-MOSFET. The high channel potential of the PSG-MOSFET enables effective blocking of drain leakage current until avalanche breakdown occurs. Therefore, the PSG-MOSFET exhibits superior breakdown characteristics compared to the SG-MOSFET, due to the P-shielding region which protects the gate oxide from the electric field.

However, the expansion of the depletion region by the P-shielding region can narrow the current path of the PSG-MOSFET, which results in degraded conduction behavior. As shown in Fig. 5, the depletion region induced by the P-shielding region leads to a narrower current path for the PSG-MOSFET ($W_P = 0.3$ μm) in conduction mode in comparison to the SG-MOSFET. Furthermore, the restricted current path within the JFET region of the PSG-MOSFET also results in a 13.72% increase $R_{on,sp}$ in comparison to the SG-MOSFET. Therefore, it is crucial to optimize the W_P by considering the trade-off between the blocking capability and the conduction behavior.

Figure 6a, b show the comparative analysis of the BV, $E_{ox,max}$, and $R_{on,sp}$ characteristics according to the W_P. A W_P of 0.0 μm refers to the SG-MOSFET. As shown in Fig. 6a,

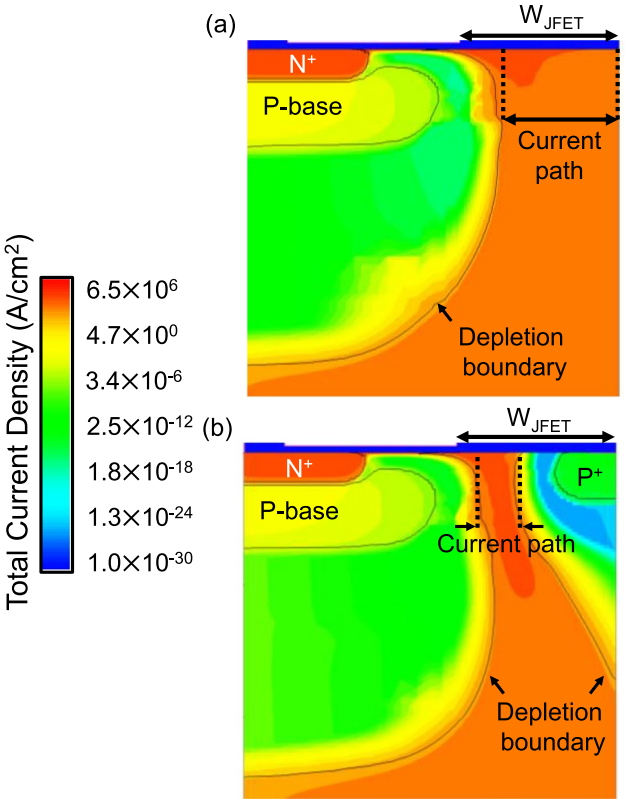

Fig. 5 Total current density in conduction mode (at a V_{DS} of 20 V and a V_{GS} of 18 V) for the **a** SG-MOSFET and **b** PSG-MOSFET

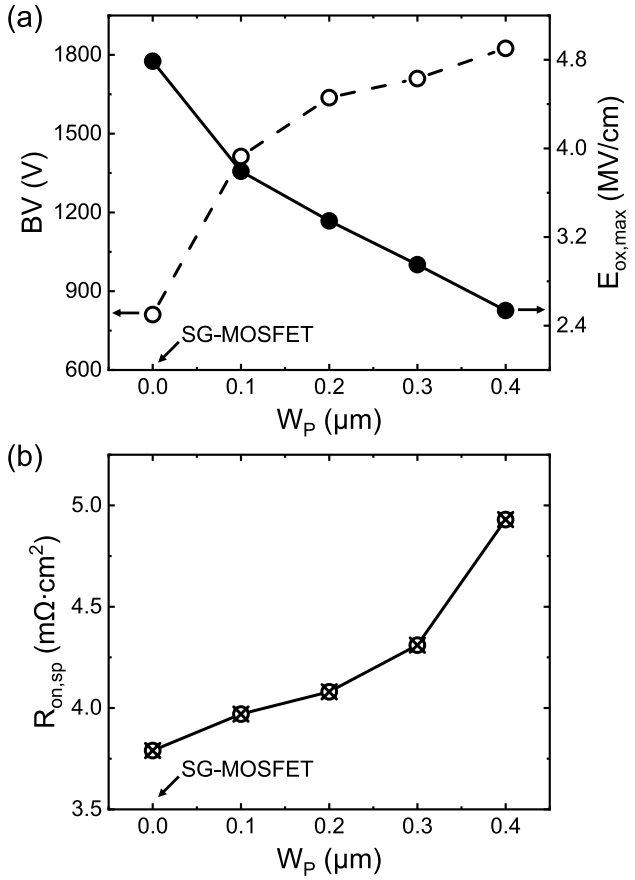

Fig. 6 Comparison of the **a** BV, $E_{ox,max}$ and **b** $R_{on,sp}$ characteristics according to the W_P

the $E_{ox,max}$ is inversely proportional to the W_P. As the W_P increases, the $E_{ox,max}$ decreases due to further suppression of the electric field crowding at the gate oxide. However, an increased W_P results in a narrowing of the current path within the JFET region, which subsequently leads to a higher $R_{on,sp}$, as shown in Fig. 6b. In particular, it is observed that when the W_P increases from 0.3 μm to 0.4 μm, the $R_{on,sp}$ increases dramatically by 14.39%, from 4.31 mΩ·cm^2 to 4.93 mΩ·cm^2. A W_P of 0.3 μm was identified as optimal value, balancing the trade-off between the blocking capability and the conduction behaviors. Under the optimized condition with a W_P of 0.3 μm, a $R_{on,sp}$ of 4.31 mΩ·cm^2, a BV of 1710 V, and an $E_{ox,max}$ of 2.95 MV/cm were achieved.

Figure 7 shows the comparative analysis of $R_{on,sp}$ and $E_{ox,max}$ of SG-MOSFETs and PSG-MOSFETs according to the L_{PJ}. For both devices, the $R_{on,sp}$ is inversely proportional to the L_{PJ}. When the L_{PJ} of both devices exceeds 0.3 μm, the saturation in the change in $R_{on,sp}$ is observed. Conversely, the $E_{ox,max}$ is proportional to the L_{PJ}. However, it is observed that misalignment of the split poly-Si gate has a considerable impact on the $E_{ox,max}$ for SG-MOSFETs. Specifically, when

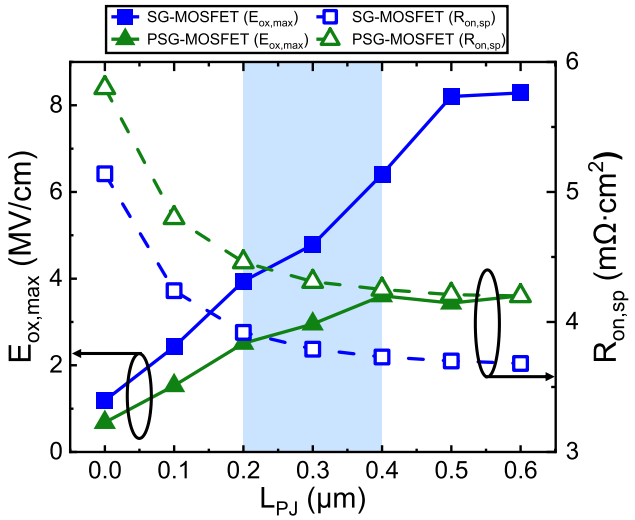

Fig. 7 Comparison of the $R_{on,sp}$ and $E_{ox,max}$ for SG-MOSFETs and PSG-MOSFETs according to the L_{PJ}

the L_{PJ} is 0.5 µm or greater, SG-MOSFETs exhibit an $E_{ox,max}$ exceeding 8 MV/cm, which is the critical electric field for SiO_2 [39]. In contrast, for PSG-MOSFETs, it is shown that the $E_{ox,max}$ remains at a reliable level even when L_{PJ} varies due to the P-shielding region which can protect the gate oxide from the electric field.

The parasitic capacitance characteristics of 1.2 kV SiC MOSFETs were extracted at a test frequency of 1 MHz via mixed-mode simulation as shown in Fig. 8. It is noted that the PSG-MOSFET exhibits a significantly reduced C_{rss} in comparison to both the C-MOSFET and the SG-MOSFET. Specifically, at a V_{DS} of 1 kV, the C_{rss} of the PSG-MOSFET was reduced by 85.71% and 55.32% in comparison to the C- MOSFET and the SG-MOSFET, respectively. As shown in Eq. (1) and Fig. 9a, the C_{rss} is the series-connected capacitance of the C_{ox} and C_{dep}. For the SG-MOSFET and PSG-MOSFET, the reduction in C_{ox} can be achieved by the split gate structure. As shown in Fig. 9b, the further expansion of the depletion region by the P-shielding region is responsible for the significant reduction in the C_{dep}. As a result of the reduction in both the C_{ox} and the C_{dep}, the C_{rss} of the PSG-MOSFET can be considerably reduced in comparison to that of the C-MOSFET and SG-MOSFET. In contrast, the input capacitance (C_{iss}) and output capacitance (C_{oss}) of the PSG-MOSFET exhibit only a negligible change.

$$C_{rss} = C_{GD} = \frac{C_{ox} \times C_{dep}}{C_{ox} + C_{dep}} \quad (1)$$

According to Eq. (2), the Q_{GD} represents the quantity of charge that is stored in the C_{rss} during the switching process of the SiC MOSFET. In other words, a reduction in the C_{rss} is accompanied by a corresponding decrease in the Q_{GD}. The gate charge characteristics of 1.2 kV SiC MOSFETs were extracted via mixed-mode simulation, as shown in Fig. 10. It has been demonstrated that the PSG-MOSFET exhibits reduced Q_{GD}, because of improved C_{rss} in comparison to the

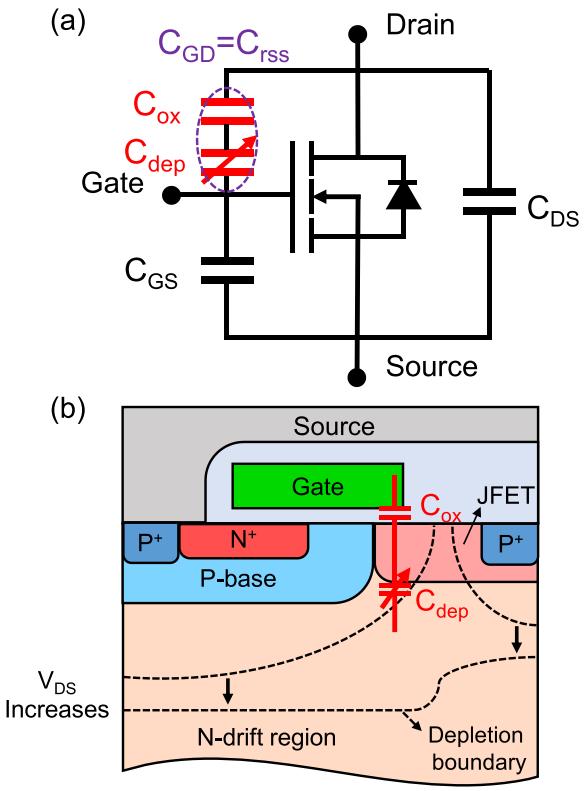

Fig. 9 **a** Parasitic capacitance within the SiC MOSFET and **b** cross-sectional view of the PSG-MOSFET in blocking mode

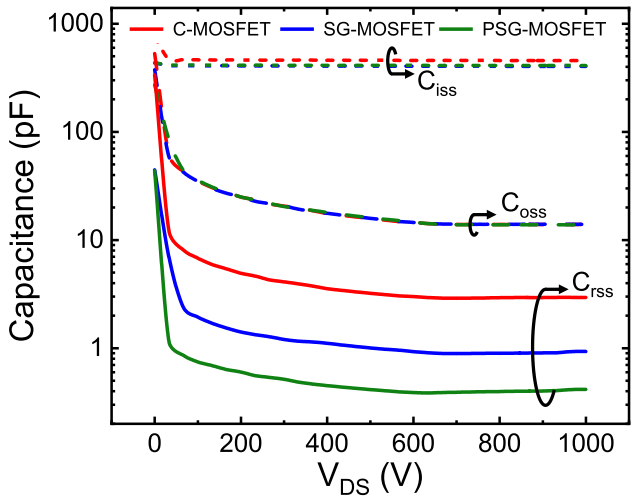

Fig. 8 Parasitic capacitance characteristics (C_{iss}, C_{oss}, C_{rss}) of 1.2 kV SiC MOSFETs

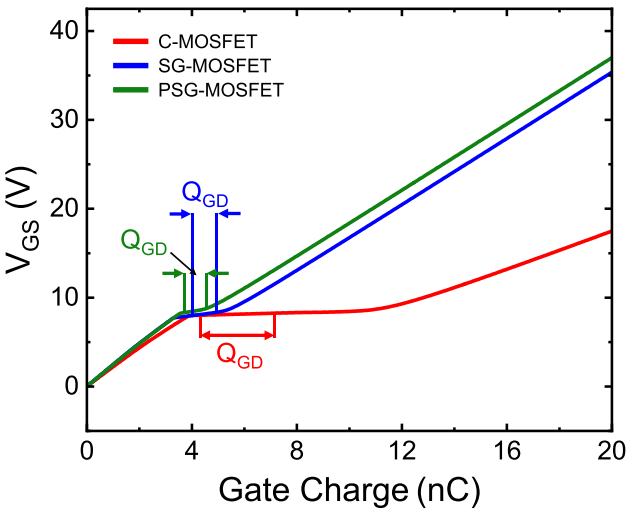

Fig. 10 Gate charge characteristics of 1.2 kV SiC MOSFETs

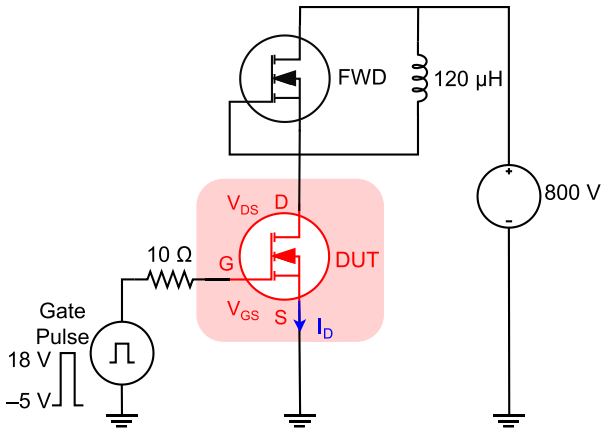

Fig. 11 Schematic of double-pulse circuit implemented in the TCAD simulation

C-MOSFET and the SG-MOSFET. Specifically, The Q_{GD} of the PSG-MOSFET is reduced by 81.85% and 47.87% in comparison to the C-MOSFET and the SG-MOSFET, respectively.

$$Q_{GD}=\int_{V_{ON}}^{V_{DS}} C_{rss}(V_D)\, dV_D \tag{2}$$

A double pulse test via mixed-mode simulation was conducted to compare the switching characteristics of 1.2 kV SiC MOSFETs. Figure 11 shows the half-bridge schematic employed in the double pulse test. The gate voltage was pulsed from − 5 V to 18 V, and an 800 V voltage source was employed at the drain stage. The internal gate resistance, external gate resistance, and load inductance were 1 mΩ, 10 Ω, and 120 µH, respectively. The total switching energy losses (E_{total}) were calculated as the sum of the turn-on switching loss (E_{on}) and the turn-off switching energy loss (E_{off}), which were extracted by integrating the product of the V_{DS} and the drain current (I_D).

Figures 12 and 13 show the switching waveforms of V_{GS}, V_{DS}, and I_D for 1.2 kV SiC MOSFETs during the turn-off and turn-on transients. As shown in Figs. 12a and 13a, the PSG-MOSFET exhibits reduced turn-off and turn-on transient times in comparison to the C-MOSFET and SG-MOSFET. Furthermore, it is noted that the PSG-MOSFET exhibits a higher *di/dt* of I_D in comparison to both structures, as shown in Figs. 12b and 13b. However, during the turn-on transient of the PSG-MOSFET, the additional reverse recovery current from the P-shield region results in a relatively large overshoot of the I_D. Nevertheless, due to the high *di/dt* and reduced turn-off and turn-on transient times, the PSG-MOSFET achieved a reduction in the E_{total} by 27.99% and 15.57%, in comparison to the C-MOSFET

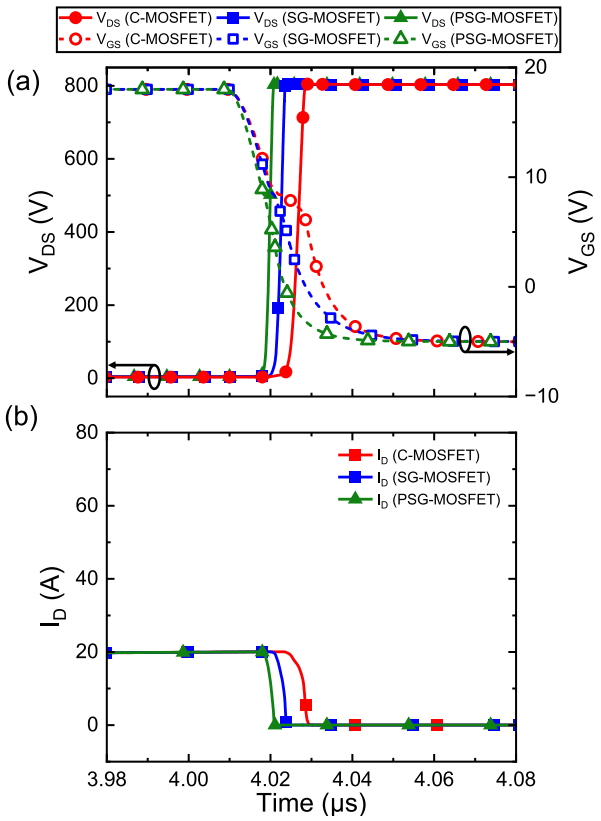

Fig. 12 Switching waveforms of the **a** V_{DS}, V_{GS}, and **b** I_D for 1.2 kV SiC MOSFETs during turn-off transient

and SG-MOSFET, respectively, as shown in Fig. 14. It is observed that this improvement in the E_{total} can be attributed to the reduced C_{rss} and Q_{GD} of the PSG-MOSFET.

Table 2 shows results of TCAD simulation conducted in this work. The $E_{ox,max}$, $R_{on,sp}$, C_{rss}, Q_{GD}, and E_{total} of the PSG-MOSFET were 2.95 MV/cm, 4.31 mΩ·cm^2, 0.49 nC, 0.42 pF, and 135.42 µJ, respectively. Although only a 13.72% increase in $R_{on,sp}$ in comparison to the SG-MOSFET, the PSG-MOSFET achieved a 38.28% decrease in $E_{ox,max}$, a 55.32% decrease in C_{rss}, a 47.85% decrease in Q_{GD}, and a 15.57% decrease in E_{total}. Consequently, the PSG-MOSFET exhibits low $E_{ox,max}$ and reduced E_{total}.

4 Conclusion

1.2 kV P-shielded Split Gate SiC MOSFETs were designed and analyzed via TCAD simulation. PSG-MOSFETs feature a P-shielding region within the JFET region to suppress the electric field crowding at the gate oxide and improve switching characteristics. The P-shielding region within the JFET region was formed through an ion implantation process for

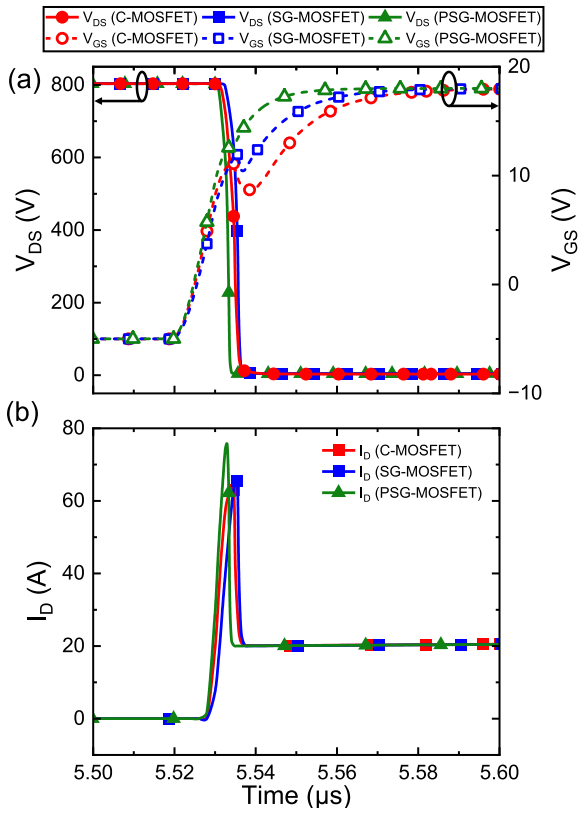

Fig. 13 Switching waveforms of the **a** V_{DS}, V_{GS}, and **b** I_D for 1.2 kV SiC MOSFETs during turn-on transient

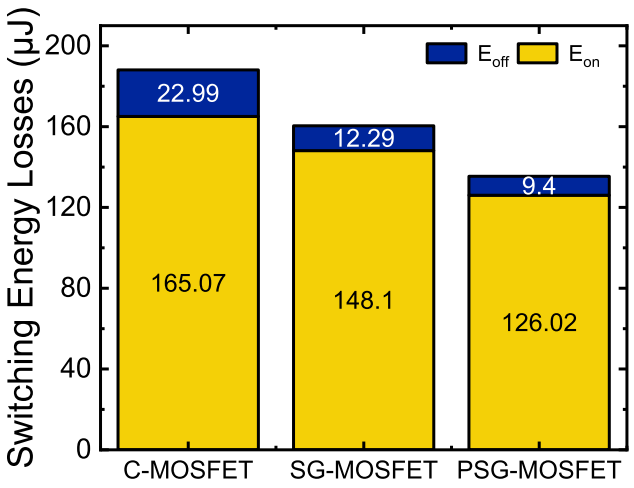

Fig. 14 Comparison of switching energy losses of 1.2 kV SiC MOSFETs

the P-source, eliminating the necessity for an additional photomask. In comparison to C-MOSFETs and SG-MOSFETs, PSG MOSFETs exhibited a reduced $E_{ox,max}$ and improved C_{rss}, Q_{GD}, and E_{total}.

Table 2 Summary of TCAD simulation results

Electrical characteristics [Unit]	C-MOSFET	SG-MOSFET	PSG-MOSFET
$R_{on,sp}$ [mΩ·cm^2]	3.65	3.80	4.31
V_{th} [V]	3.99	3.99	4.15
BV [V]	1536	811	1710
$E_{ox,max}$ [MV/cm]	4.08	4.78	2.95
Q_{GD} [nC]	2.70	0.94	0.49
C_{iss} [pF] (at V_{DS} = 1 kV)	455.57	402.82	409.94
C_{oss} [pF] (at V_{DS} = 1 kV)	13.89	13.80	13.95
C_{rss} [pF] (at V_{DS} = 1 kV)	2.94	0.93	0.42
$R_{on}\times C_{rss}$ [pΩ·F] (at V_{DS} = 1 kV)	0.72	0.24	0.12
E_{on} [μJ]	165.07	148.10	126.02
E_{off} [μJ]	22.99	12.29	9.40
E_{total} [μJ]	188.06	160.40	135.42

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Declarations

Conflict of interest Kanghee Shin, Dongkyun Kim, Minu Kim, Junho Park, and Ogyun Seok declare that we have no competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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